

CB-3 LOGIC SCHEMATICS

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034.VRAM CHANNEL-A	69.TPM	99.PTH FOR SCREW HOLES
035.BLANK	70.EEPROM/SMBUS SW	100.3rd USB

EC Modify History

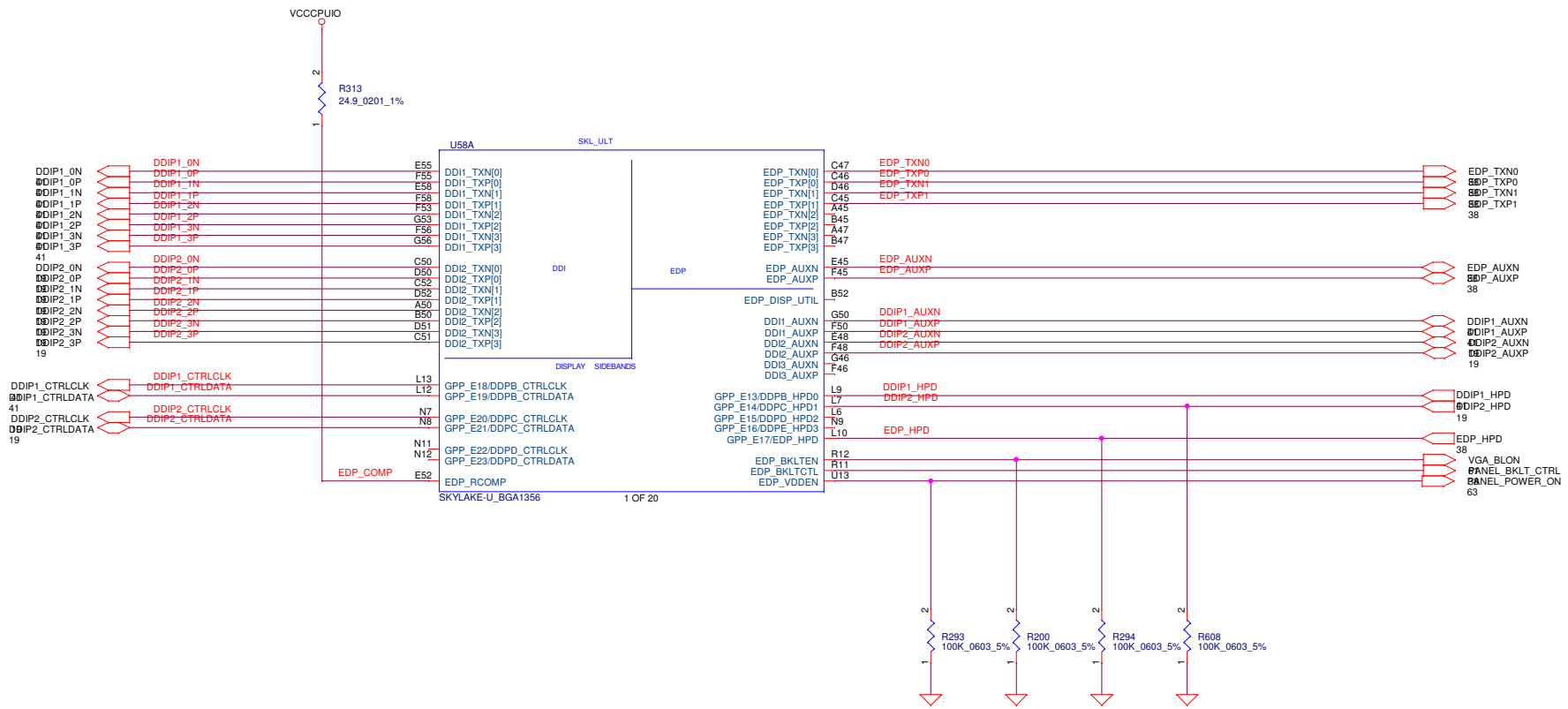
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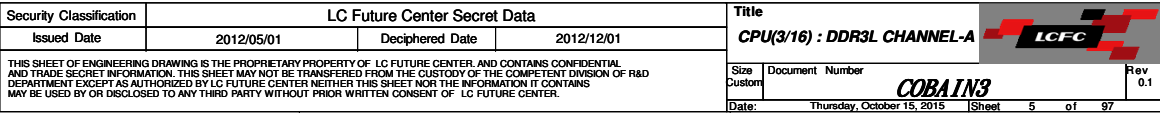
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2012/10/18	CB_1_SWG_SDV_EC016	JV_CB-1_SWG_SDV1_SCH_EC015_101701.pdf
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2012/11/27	CB_1_SWG_SDV_EC037	JV_CB-1_SWG_SDV1_SCH_EC036_112601.pdf
2012/12/05	CB_1_SWG_SDV_EC037-039	JV_CB-1_SWG_SDV_SCH_EC037-038_120401.pdf

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Issued Date	2012/05/01	Deciphered Date	2012/12/01	EC HISTORY	
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COBAN2 SWG





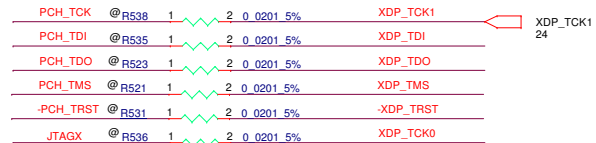
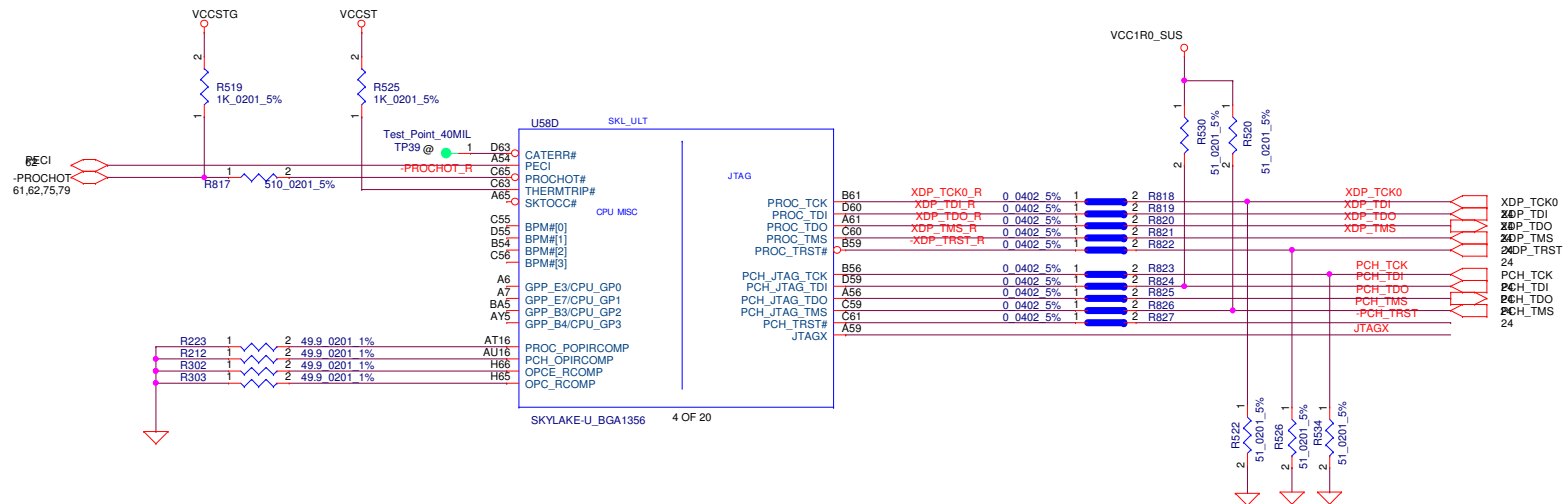


TABLE : Functional Strap

GPP_B22/GSPI0_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

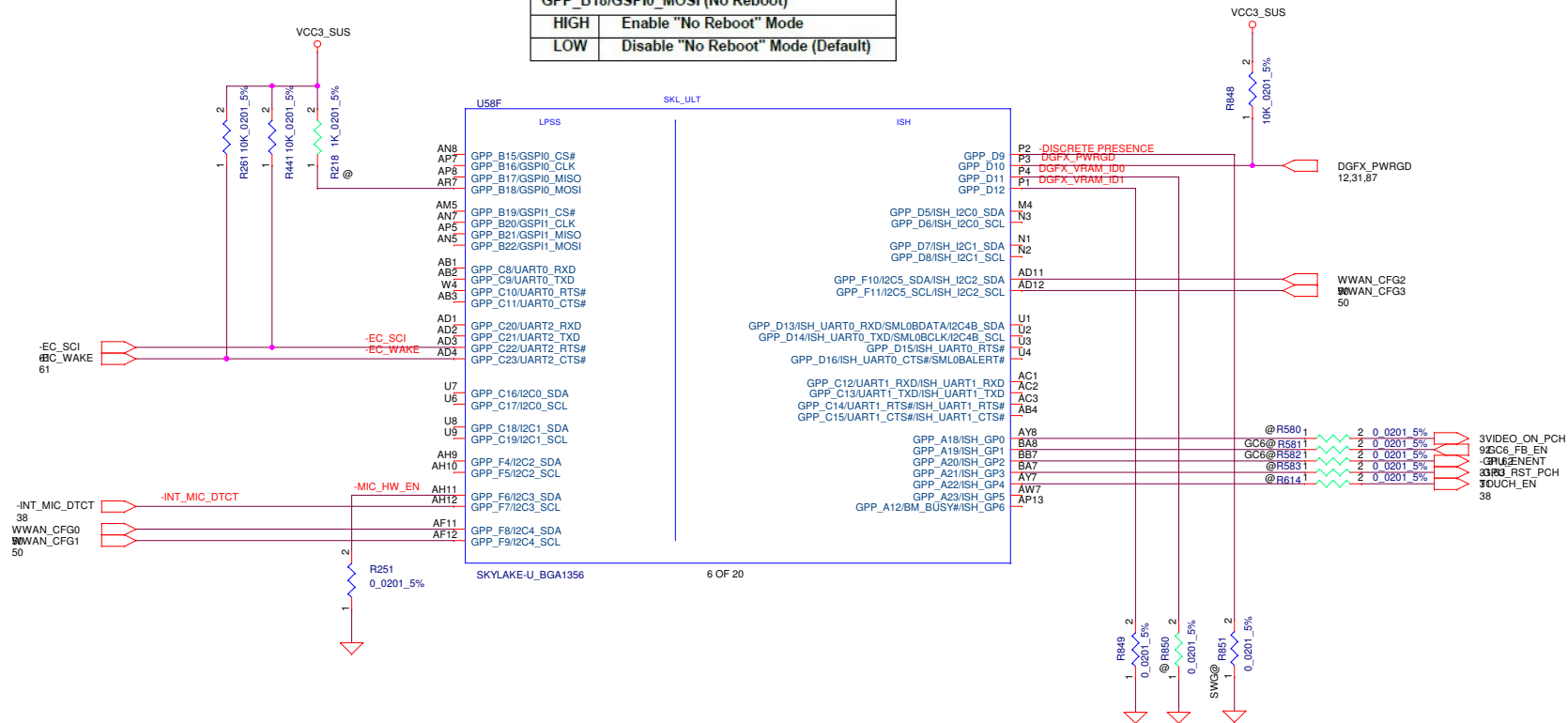
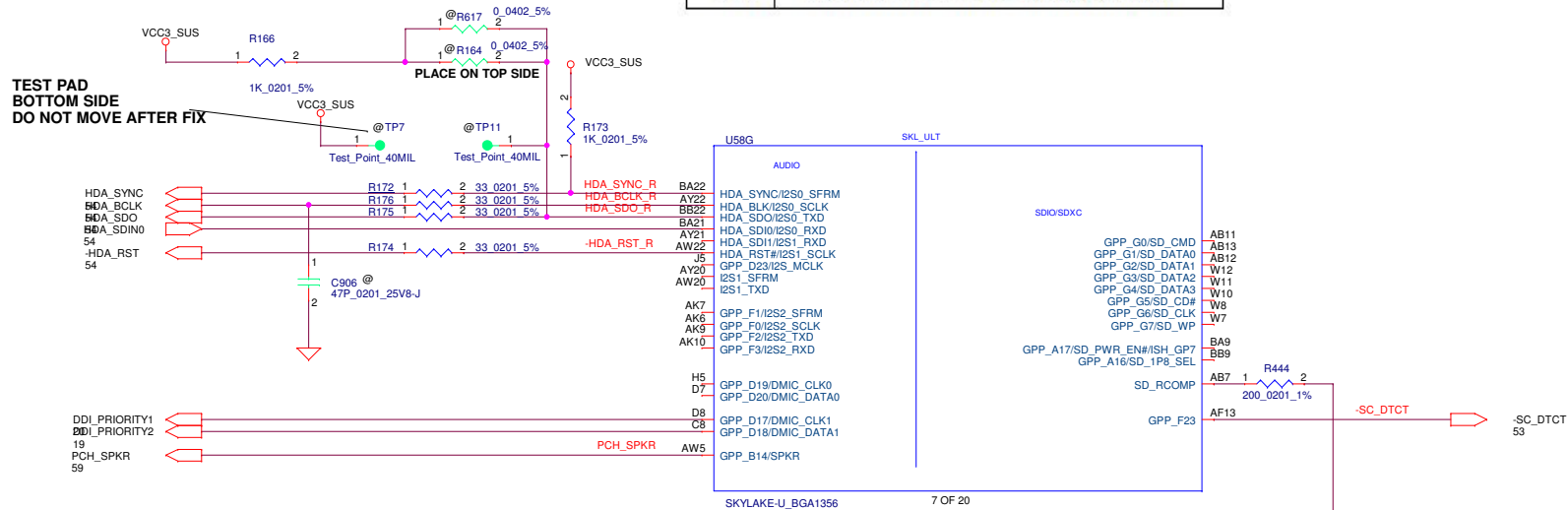


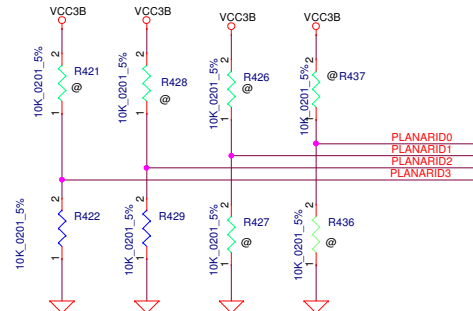
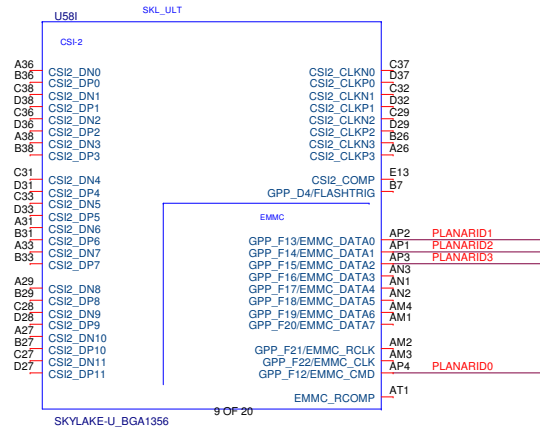
TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

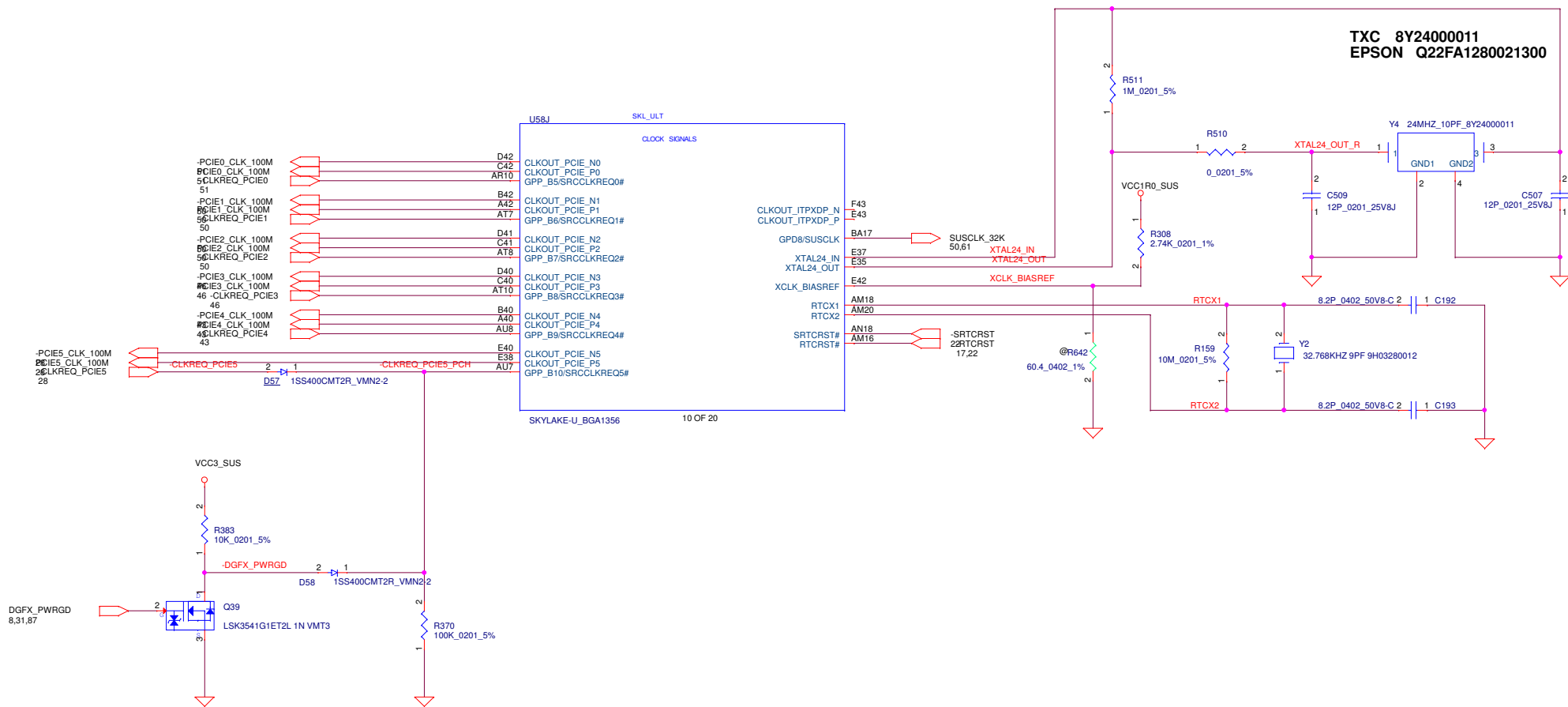


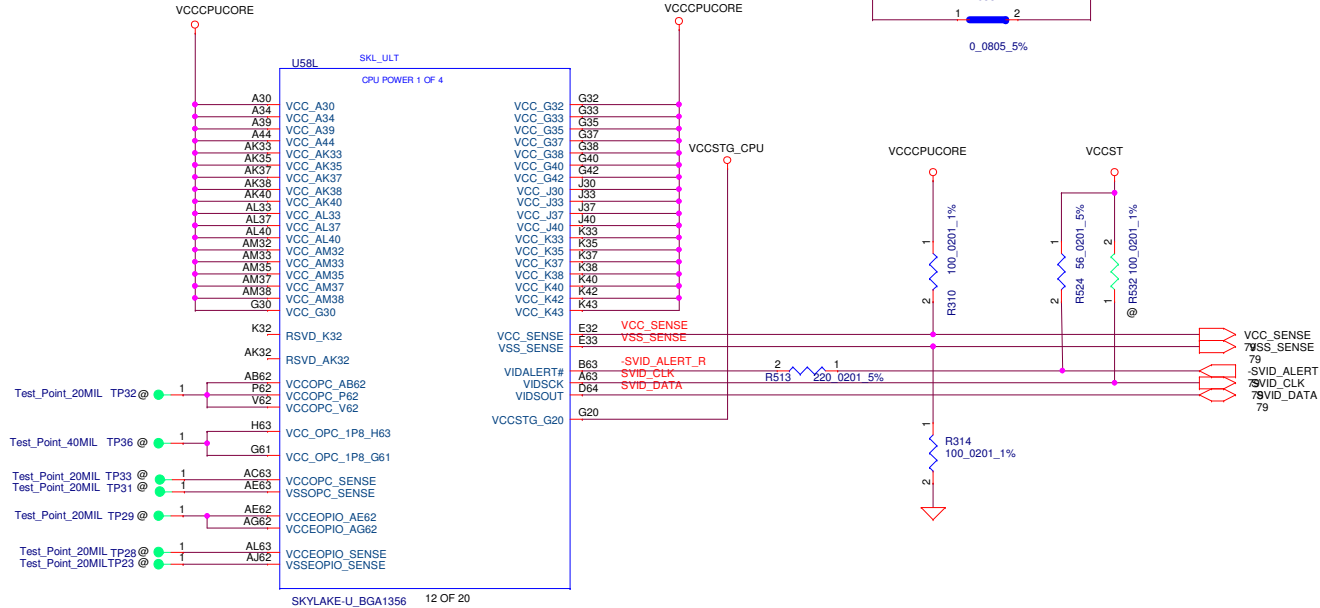
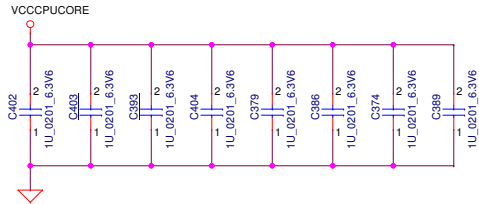
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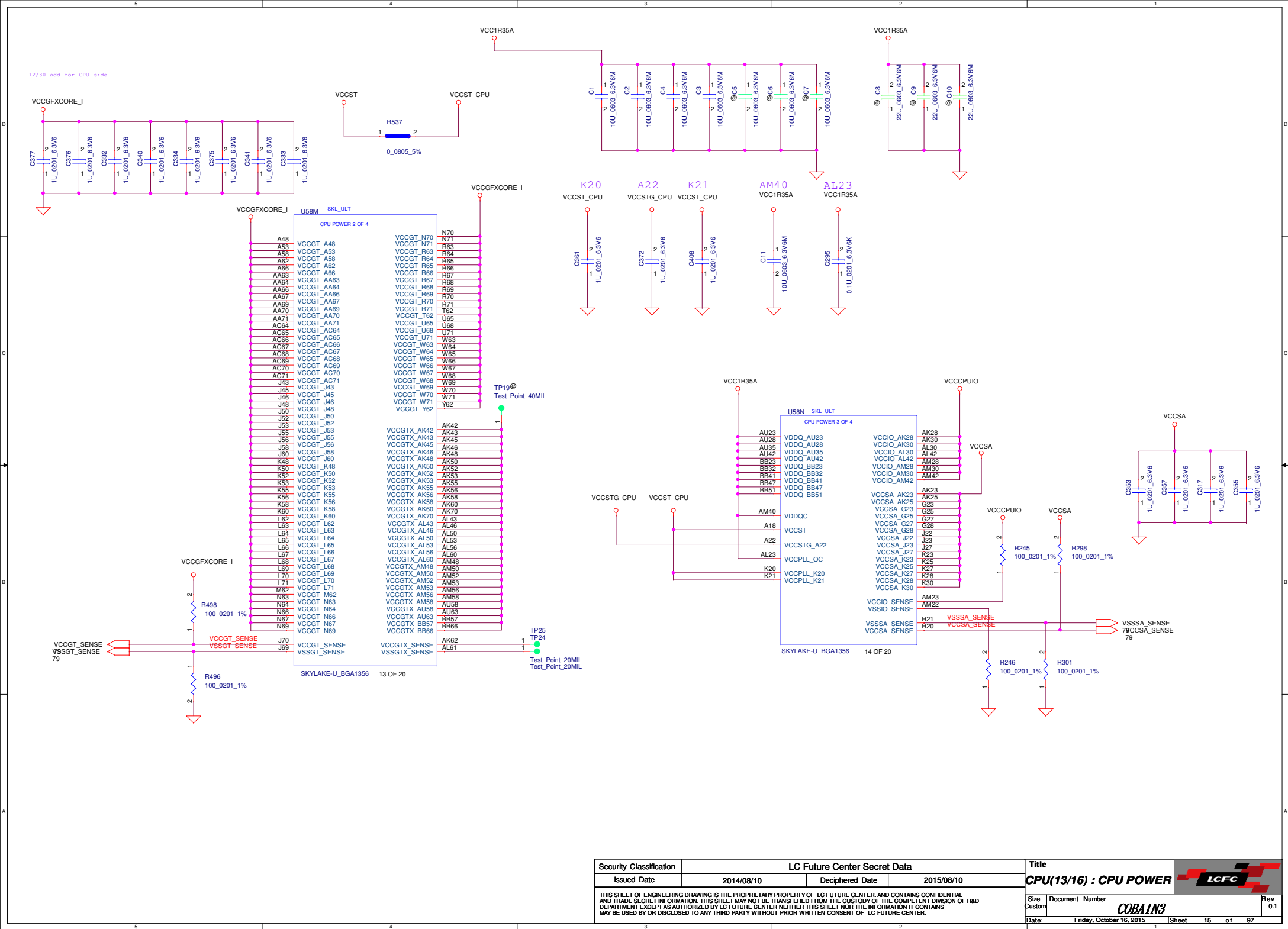
Title		LCFC	
CPU(7/16) : AUDIO/SDXC			
Size	Document	Number	Rev
Custom		COBAN3	0.1
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PLANAR ID TABLE		
LEVEL		PLANARID[3..0]
UMA	SWG	
SDV		0000B
FVT		0001B
SIT	FVT	0010B
SVT	SIT	0011B
	SVT	0100B

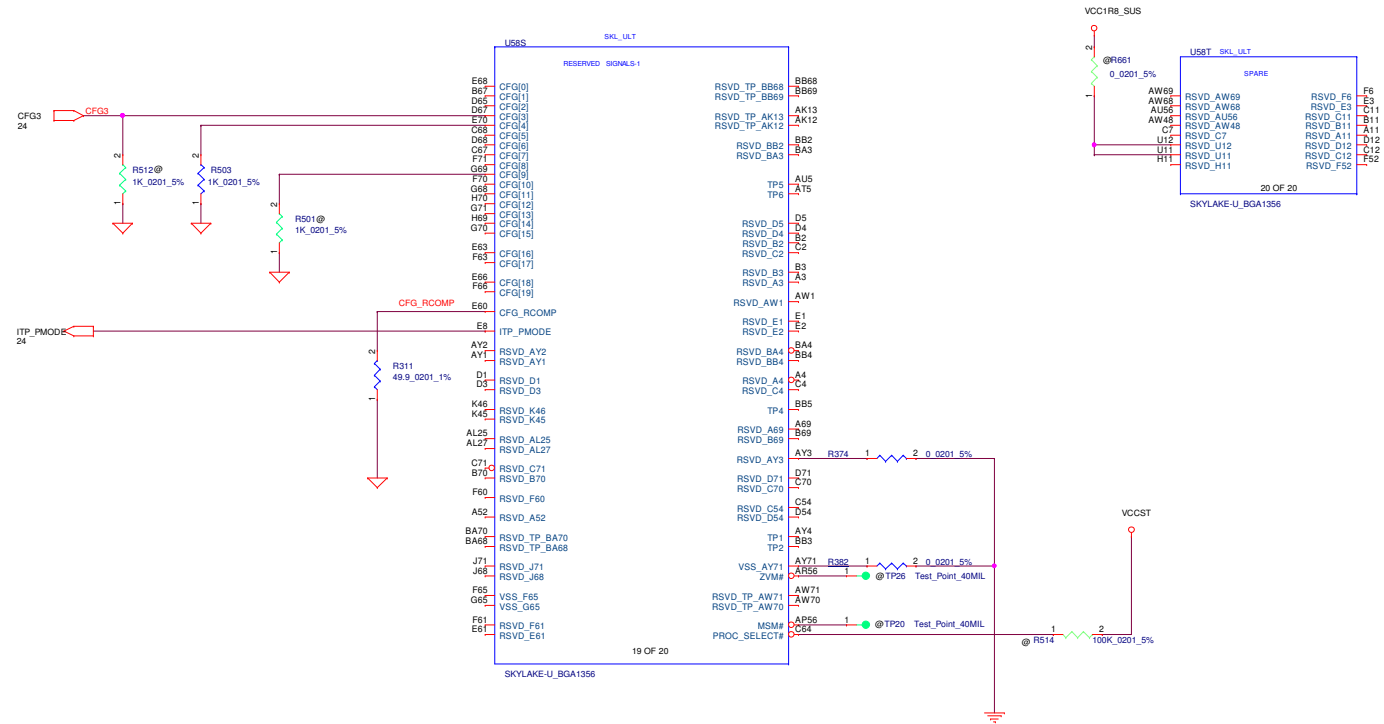





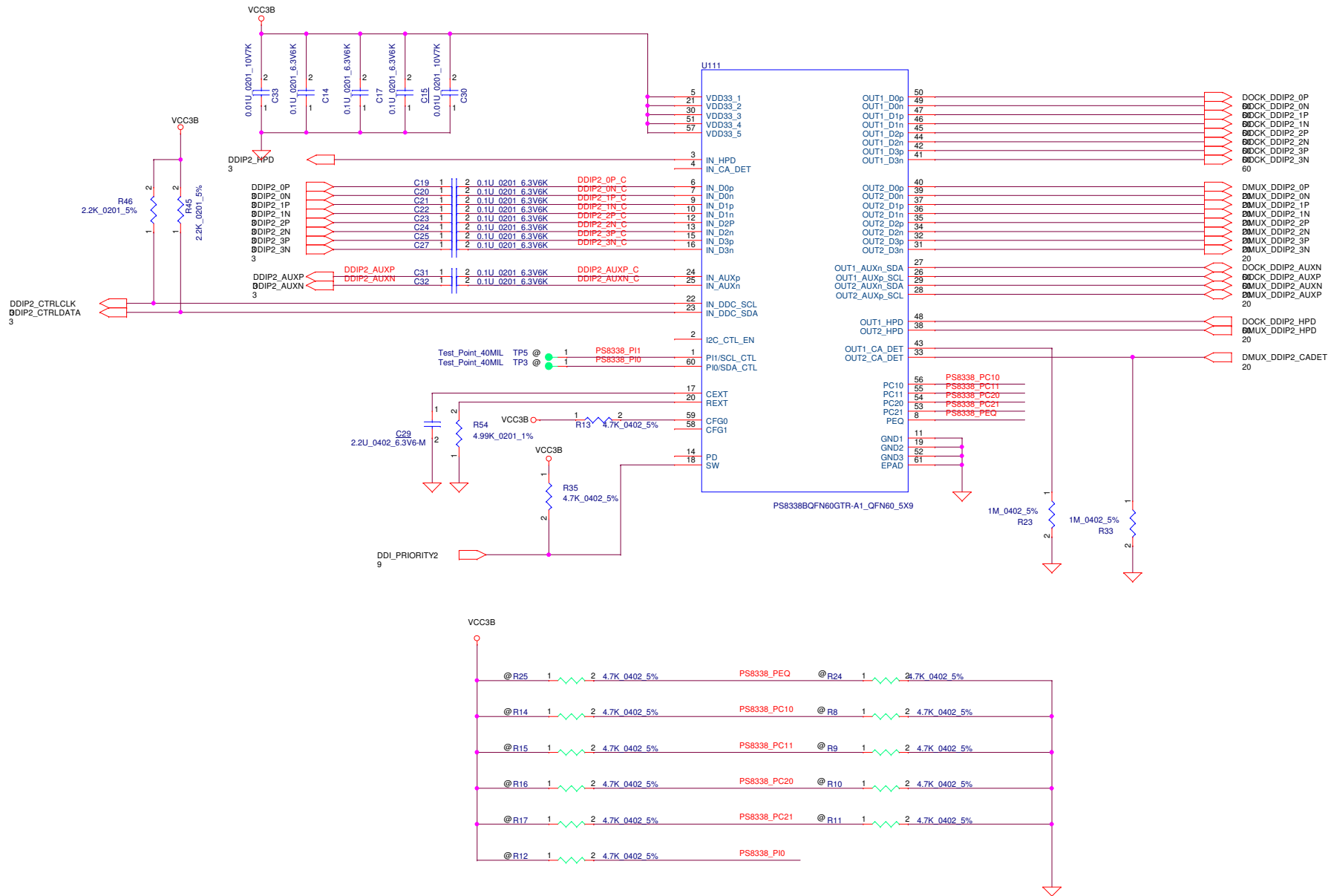


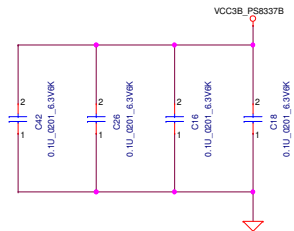
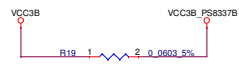
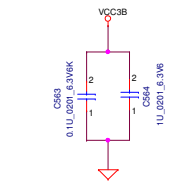
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<p>CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall</p>
<p>CFG4 : eDP Enable 1 : Disabled 0 : Enabled</p>
<p>CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled</p>

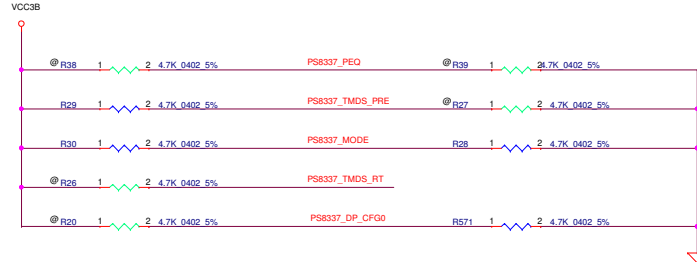
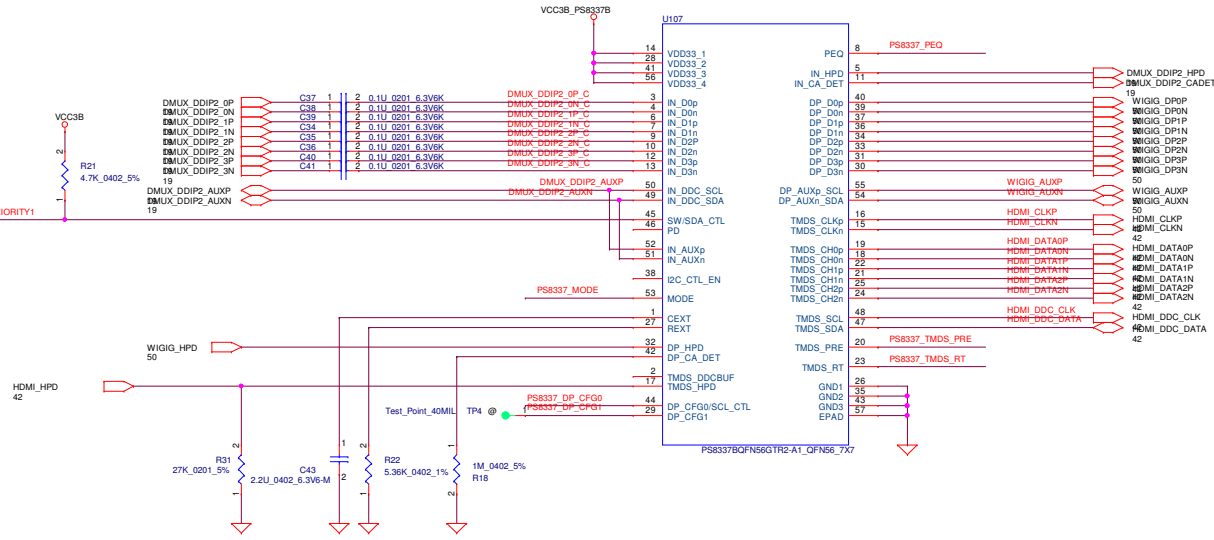


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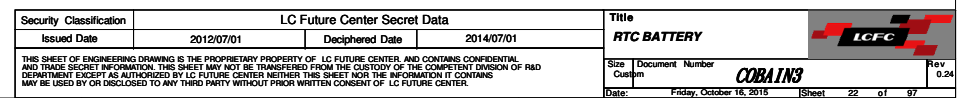


Place 0.1uF caps near each VDD33 pin of PS8337



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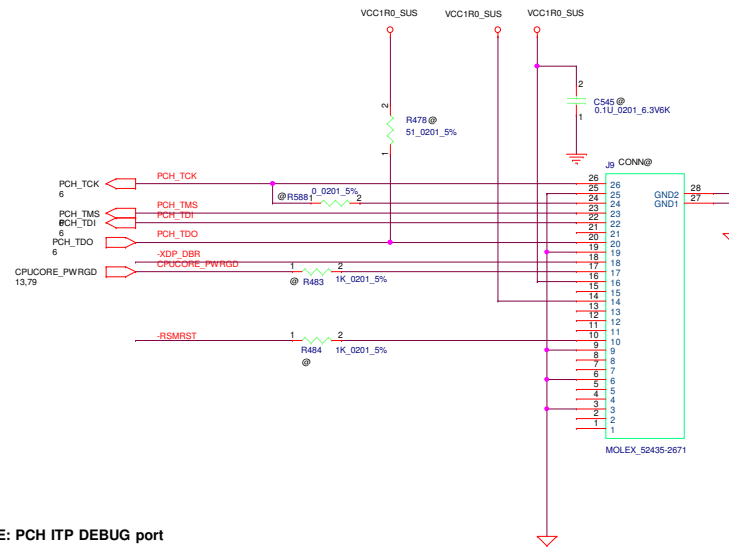
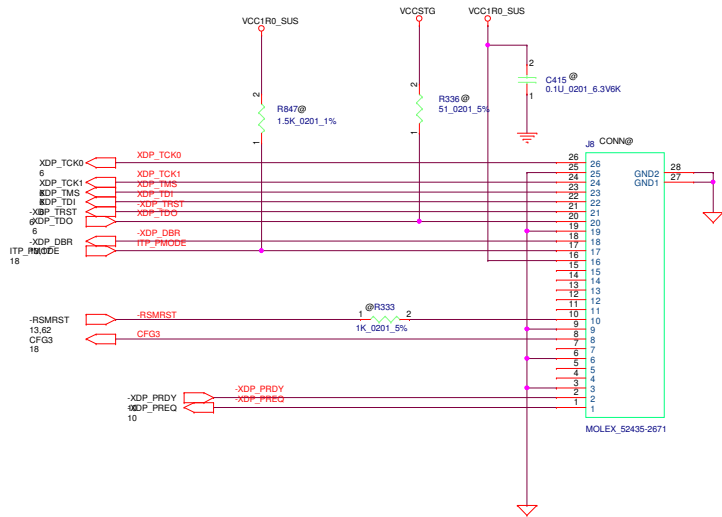
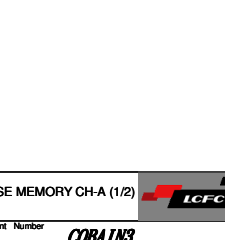
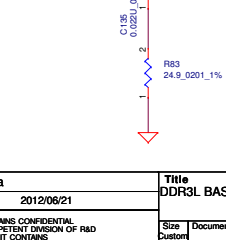
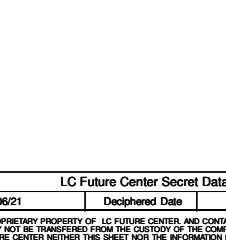
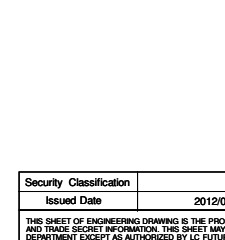
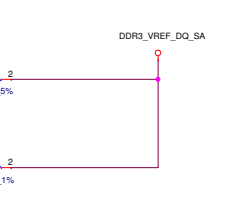
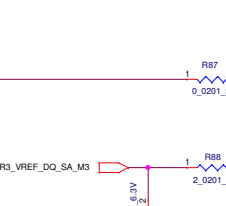
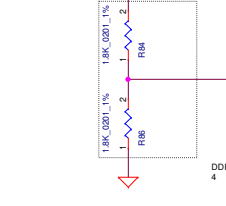
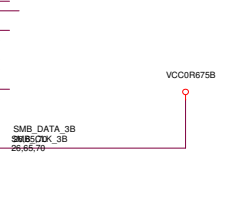
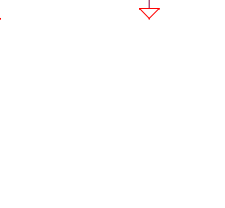
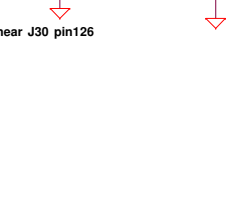
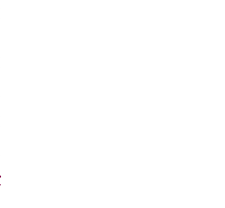
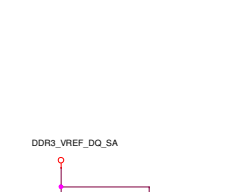
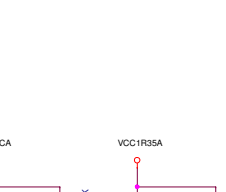
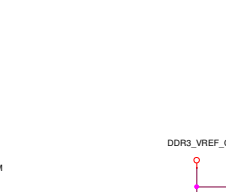
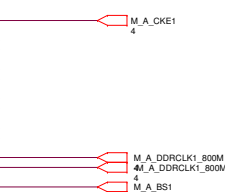
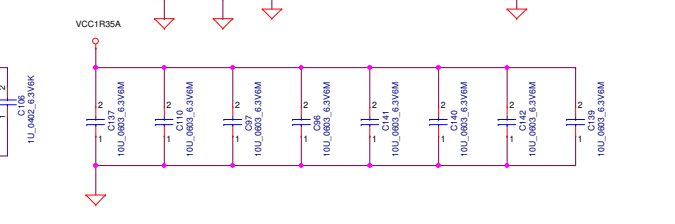
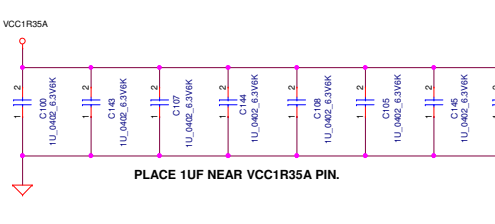
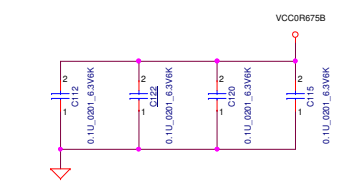
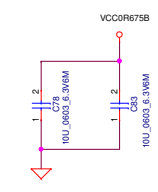
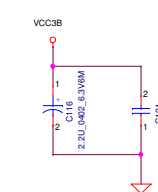
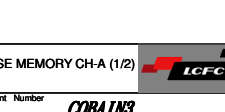
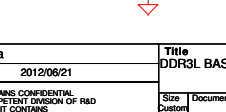
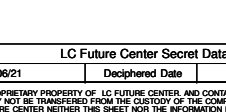
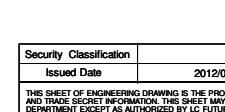
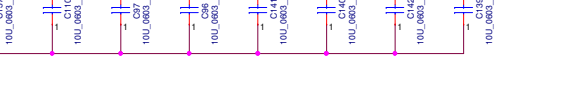
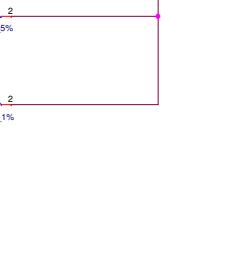
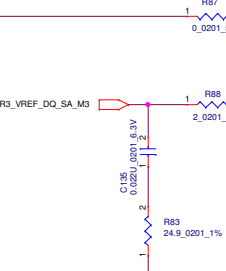
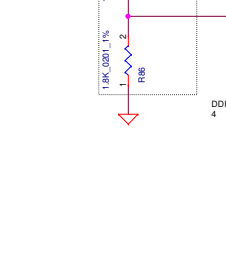
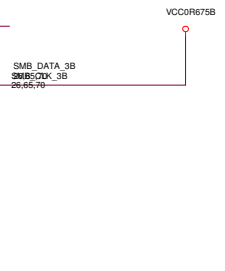
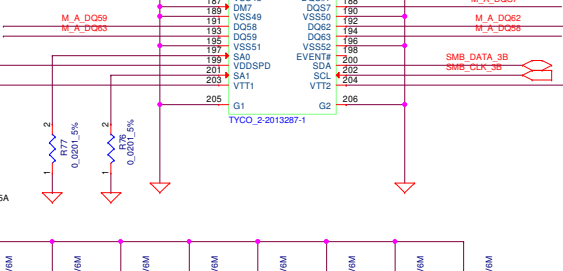
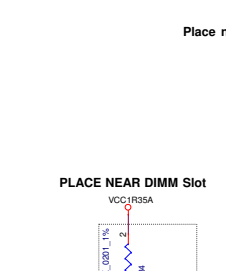
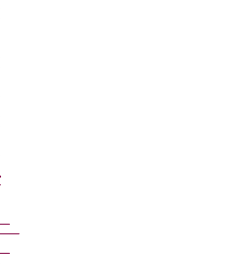
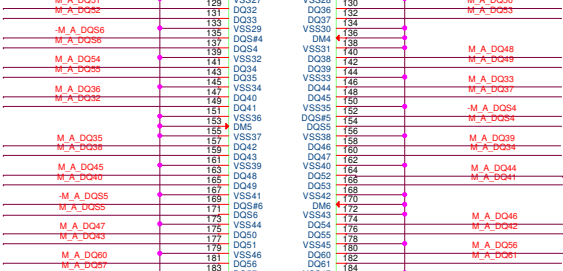
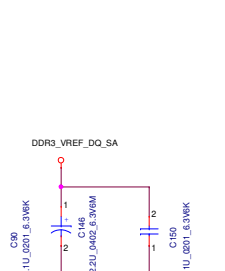
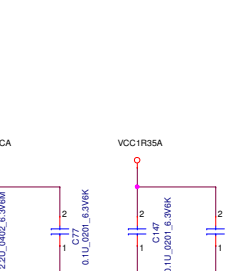
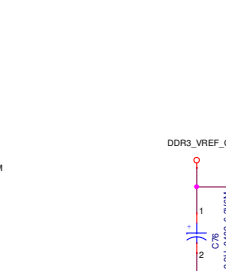
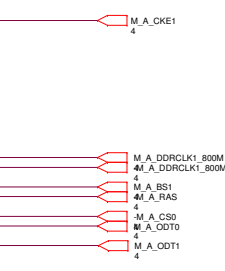
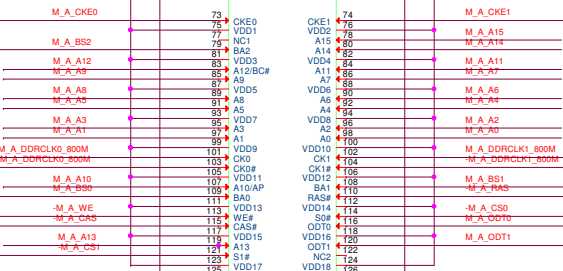
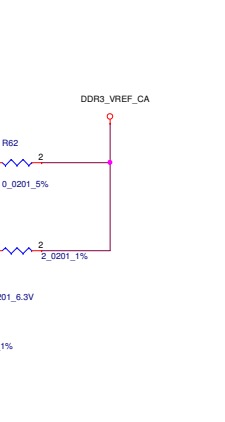
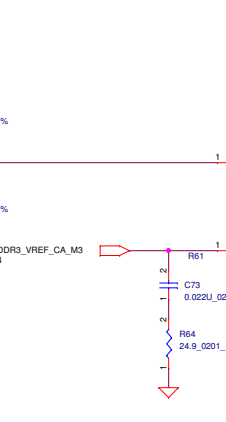
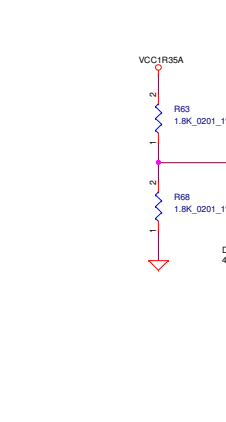
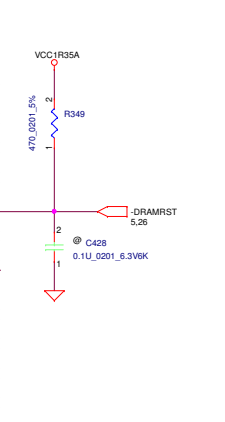
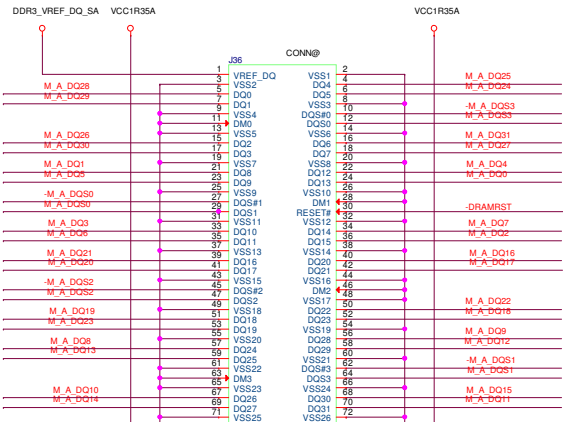
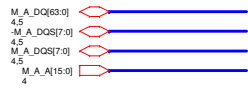



TABLE: PCH ITP DEBUG port

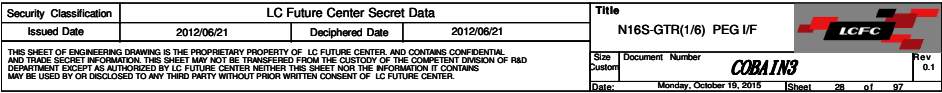
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TDO	R478 R523	ASM ASM	ASM ASM
TMS	R521	ASM	ASM
TDI	R535	ASM	ASM
TCK	R588 R538	ASM ASM	ASM ASM
CPUCORE_PWRGD	R483	ASM	ASM
-RSMRST	R484	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

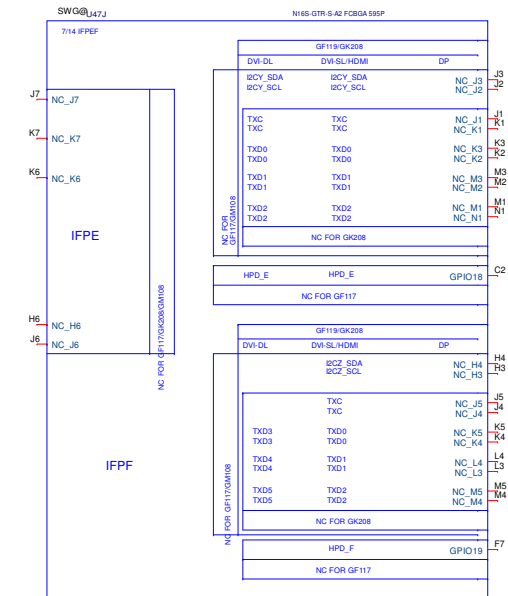
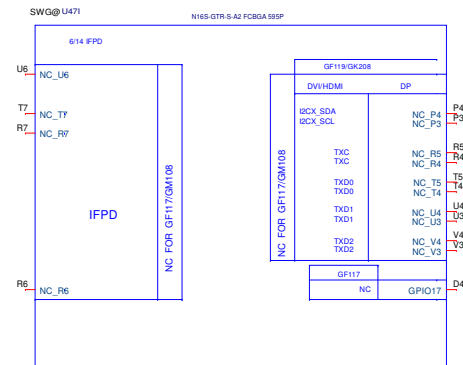
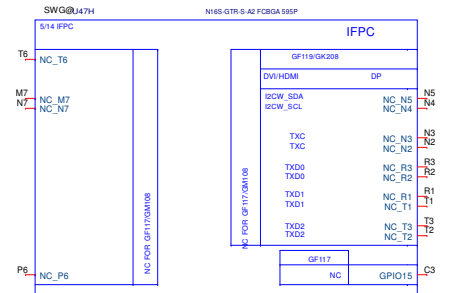
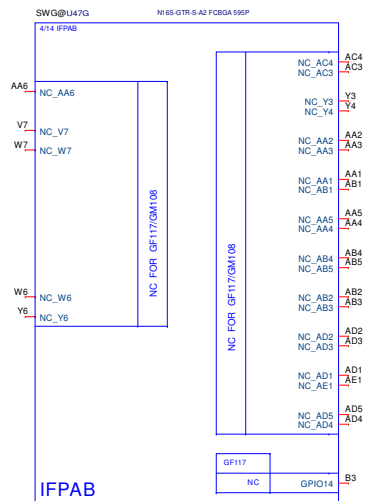
NOTE: APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

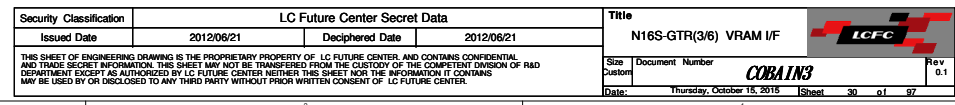


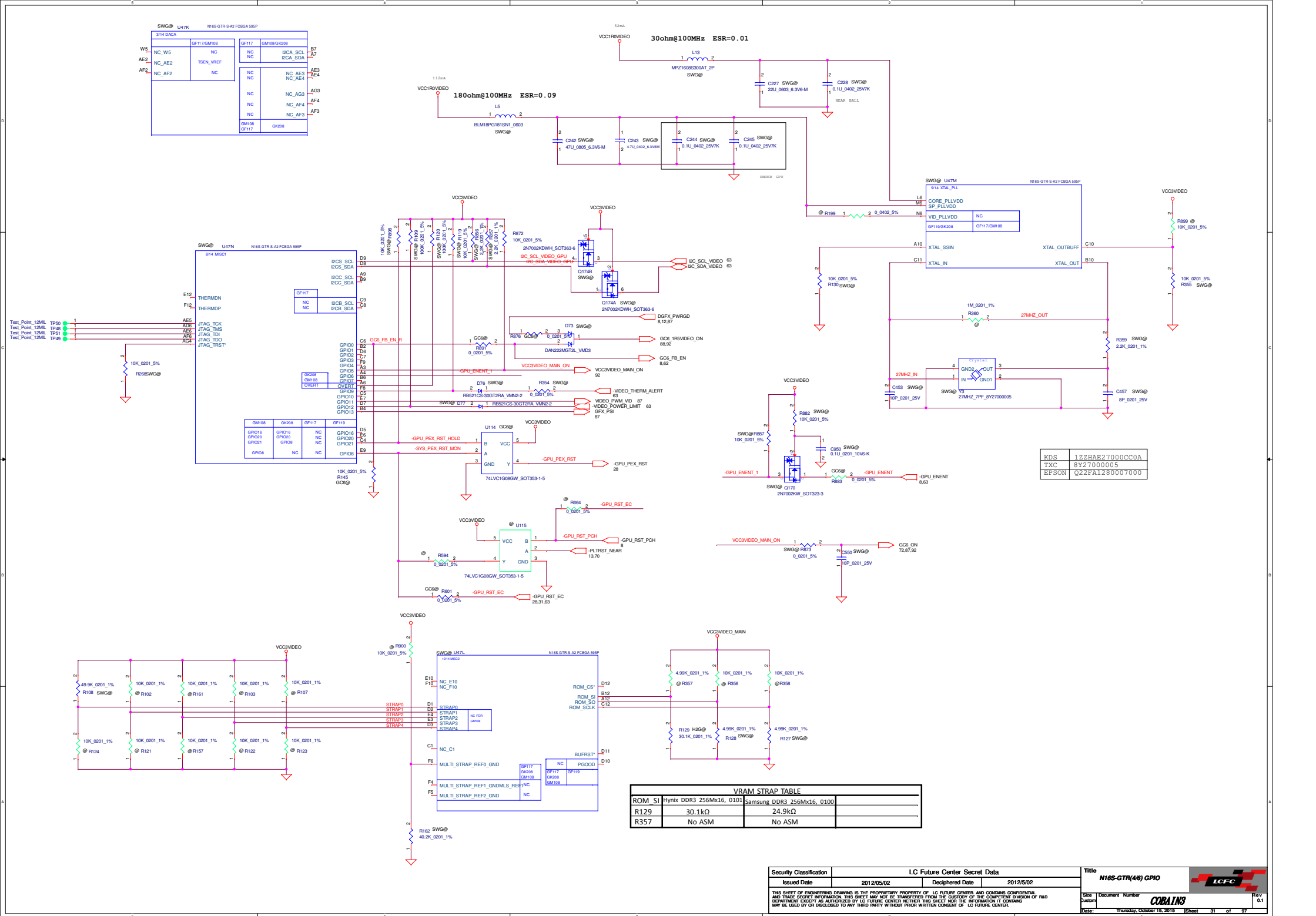
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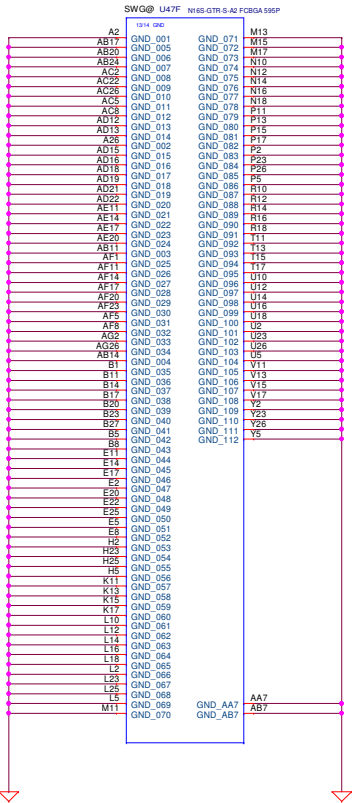
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Issued Date		Deciphered Date		DDR3L DECOUPLING	
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Custom					0.1
Date:	Thursday, October 15, 2015		Sheet	27	of 97











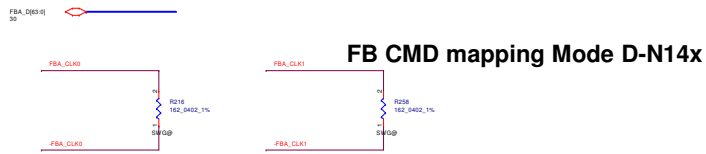
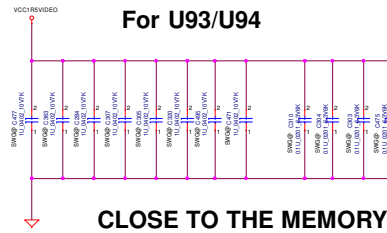
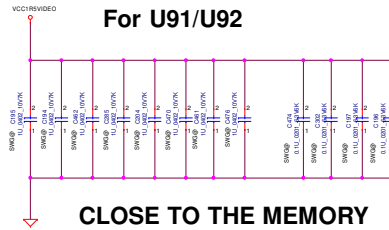
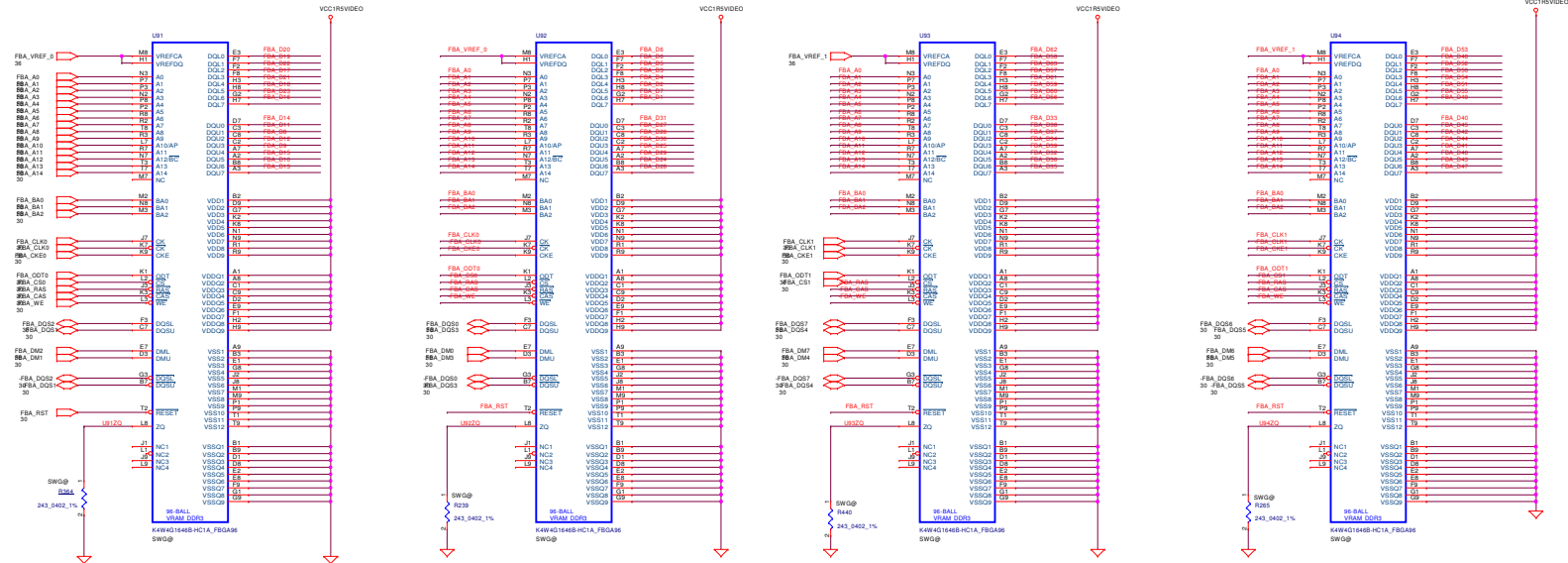


TABLE
DDR3 VIDEO MEMORY

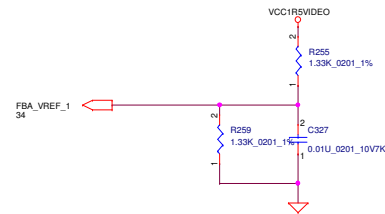
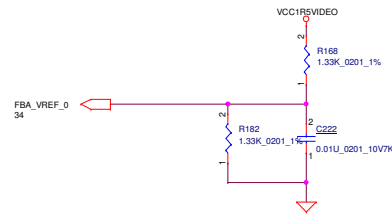
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U91 U92 U93 U94				K4W4G1646E-BC1A	H5TC4G63CFR-N0C
BOM Structure				S2G@	H2G@



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COBAIN SWG



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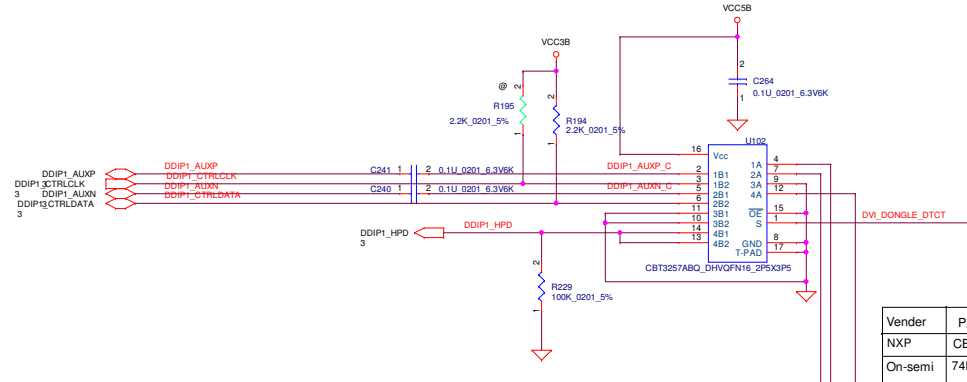
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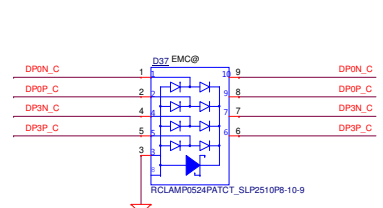
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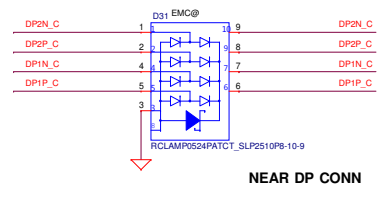


Vender	P/N
NXP	CBT3257ABQ
On-semi	74FST3257MNTWG

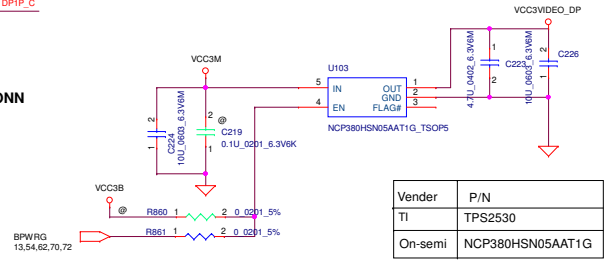
DDIP1_3N	C315	1	2	0.1U_0201_6.3V6K	DP3N_C
BDIP1_3P	C319	1	2	0.1U_0201_6.3V6K	DP3P_C
DDIP1_2N	C263	1	2	0.1U_0201_6.3V6K	DP2N_C
BDIP1_2P	C265	1	2	0.1U_0201_6.3V6K	DP2P_C
DDIP1_1N	C266	1	2	0.1U_0201_6.3V6K	DP1N_C
BDIP1_1P	C276	1	2	0.1U_0201_6.3V6K	DP1P_C
DDIP1_0N	C280	1	2	0.1U_0201_6.3V6K	DP0N_C
BDIP1_0P	C294	1	2	0.1U_0201_6.3V6K	DP0P_C



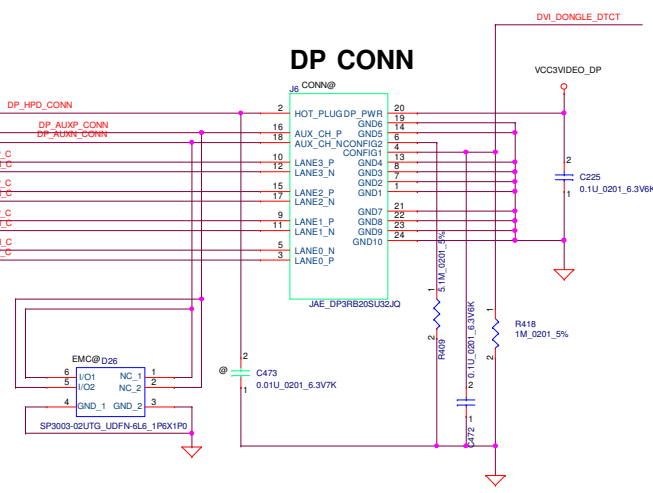
NEAR DP CONN



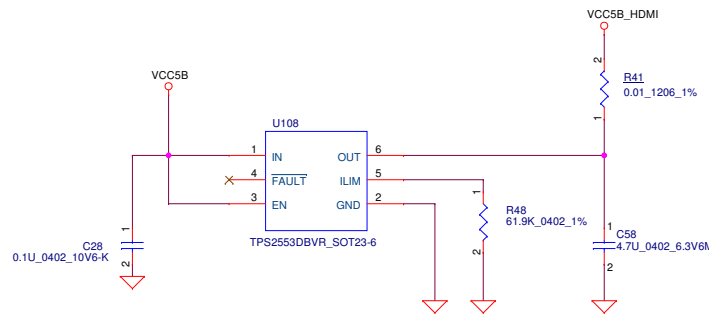
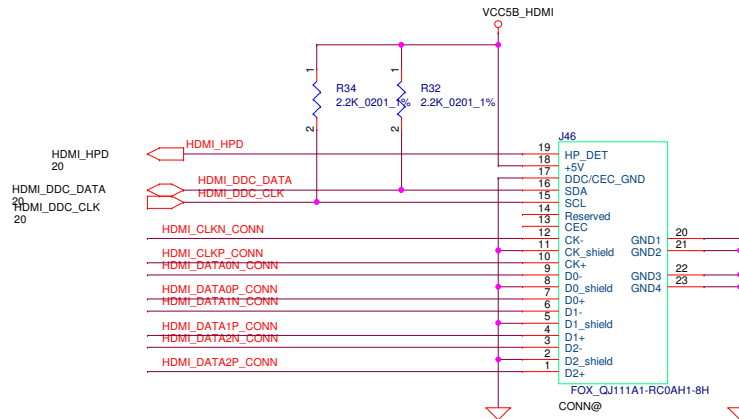
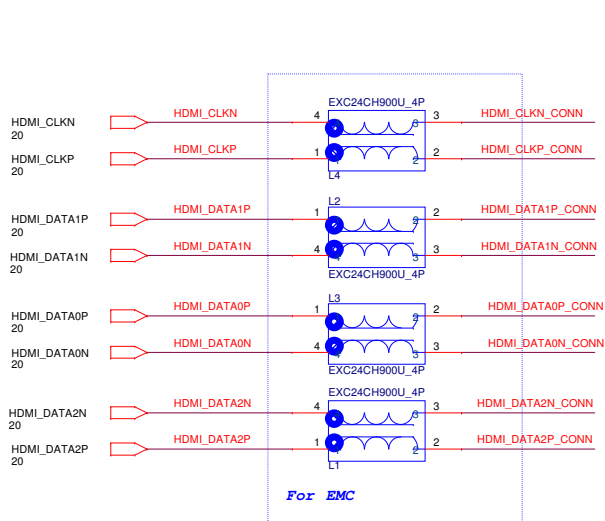
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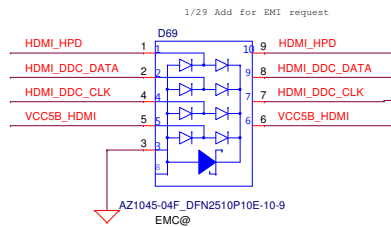
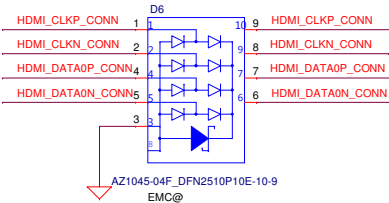
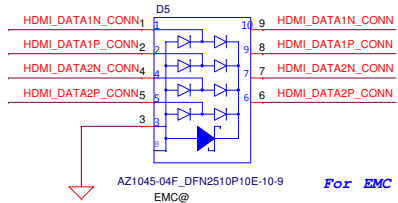
Vender	P/N
TI	TPS2530
On-semi	NCP380HSN05AAT1G



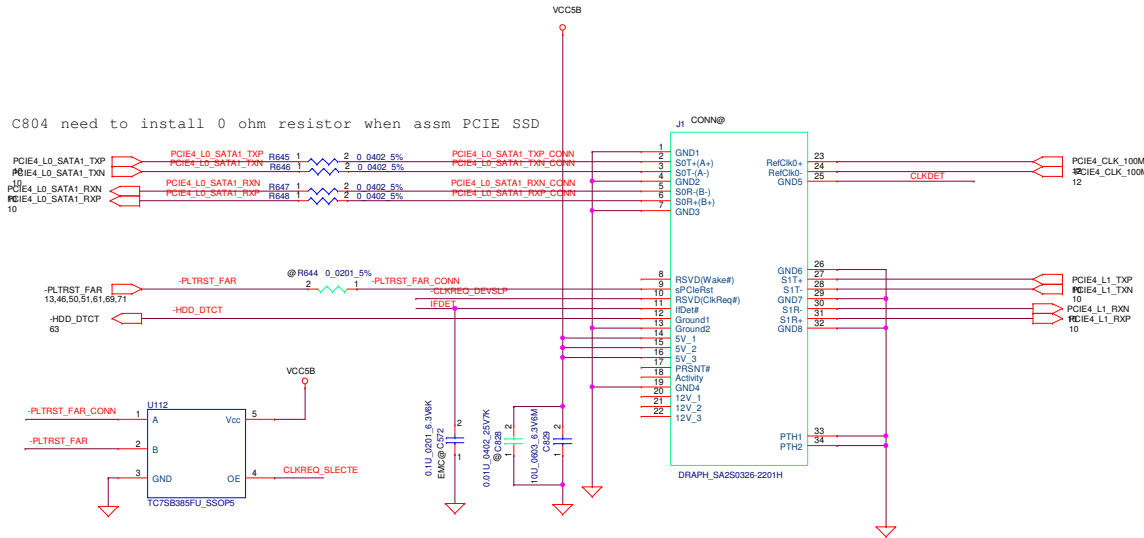
DP CONN



Close to J46

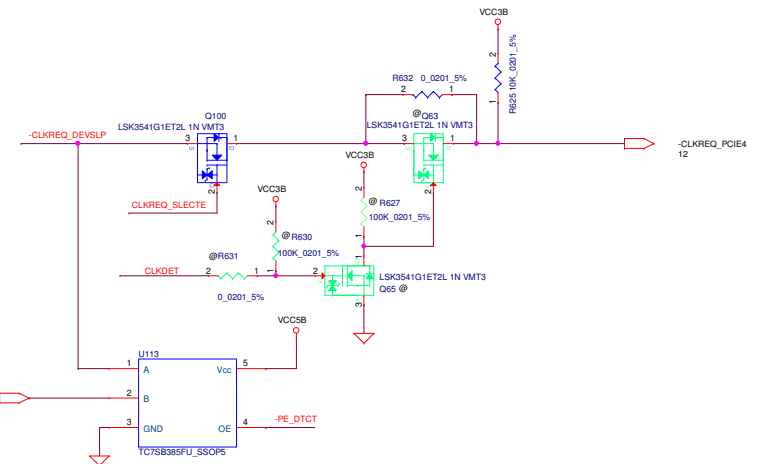
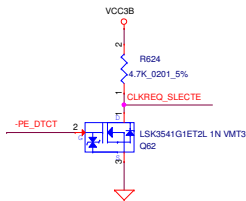
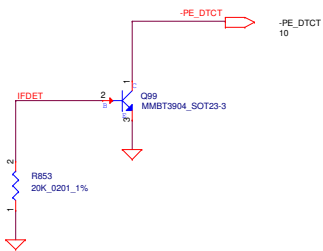


C803 and C804 need to install 0 ohm resistor when assm PCIe SSD



IFDET
SATA Device
PCIe Device

GND
5K PU to Vsource



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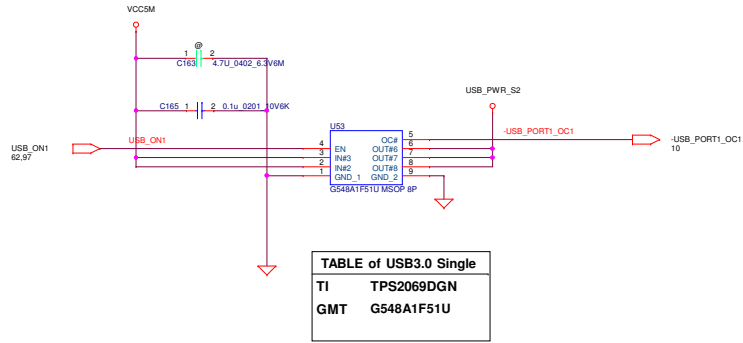
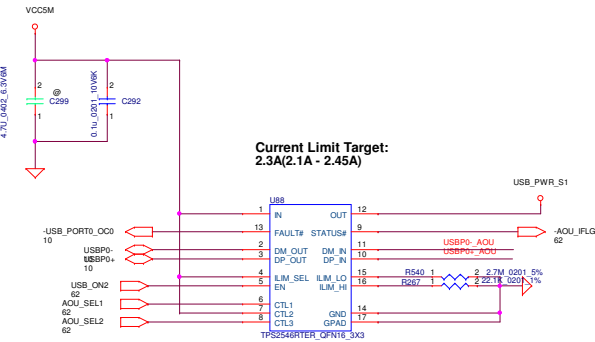
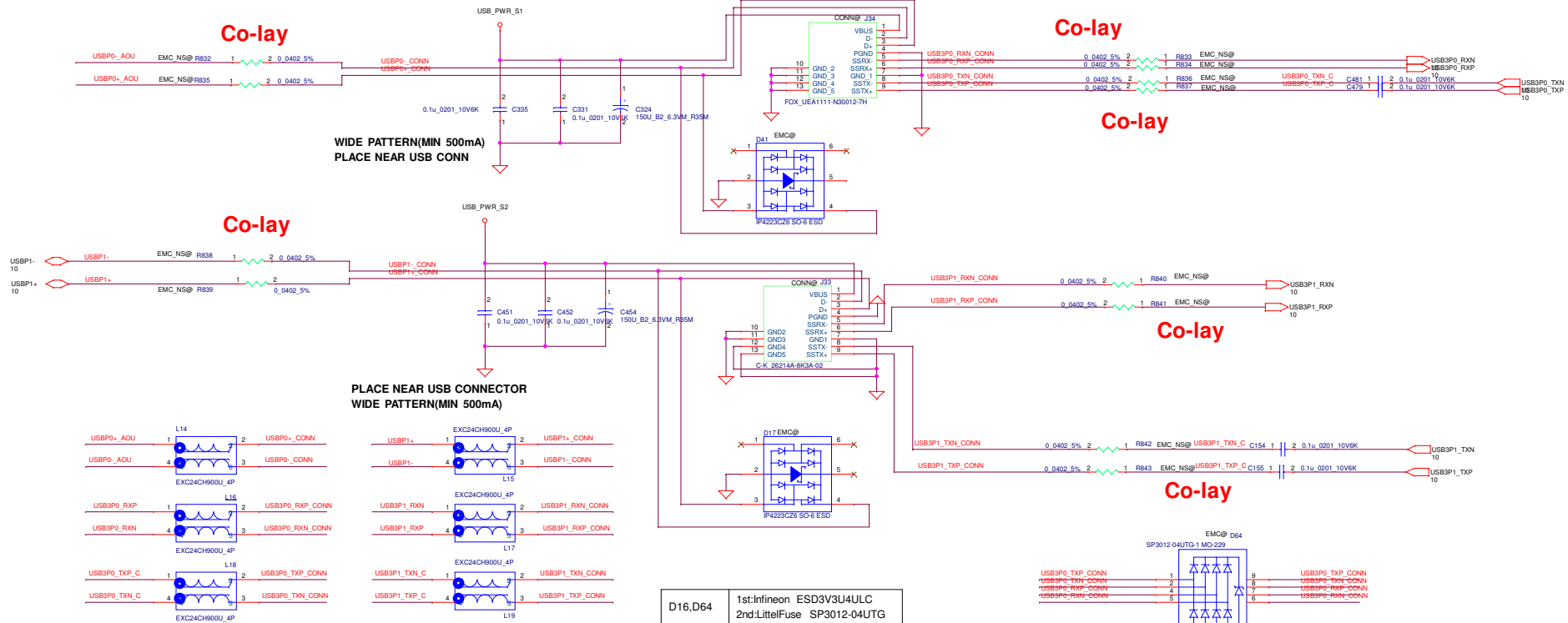
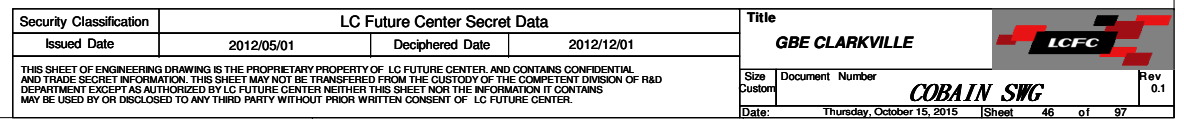
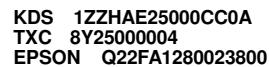
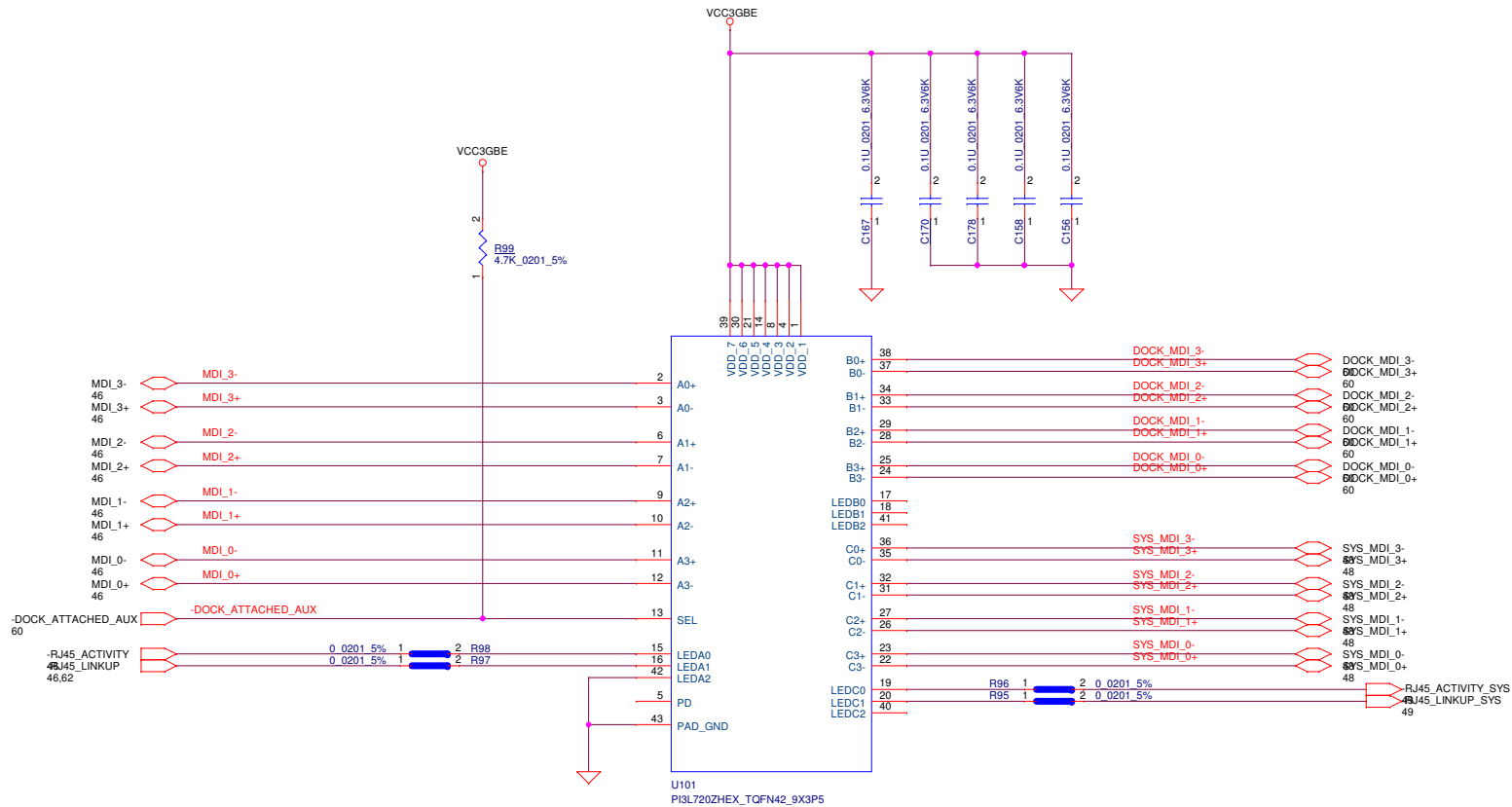


TABLE of USB3.0 Single	
TI	TPS2069DGN
GMT	G548A1F51U

Vendor	P/N
TI	TPS2546RTER



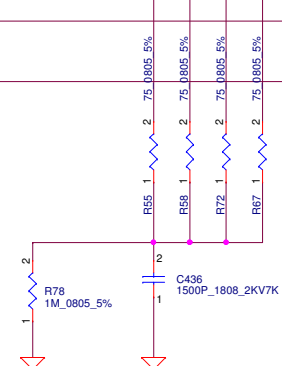
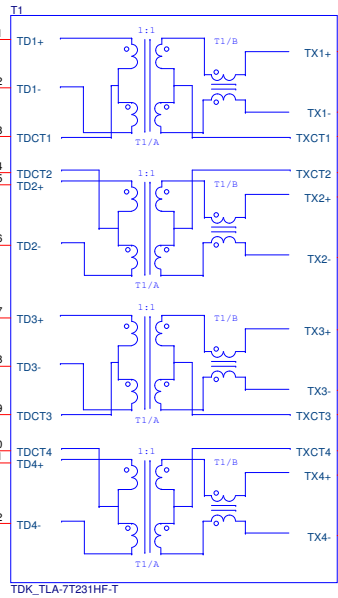


THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

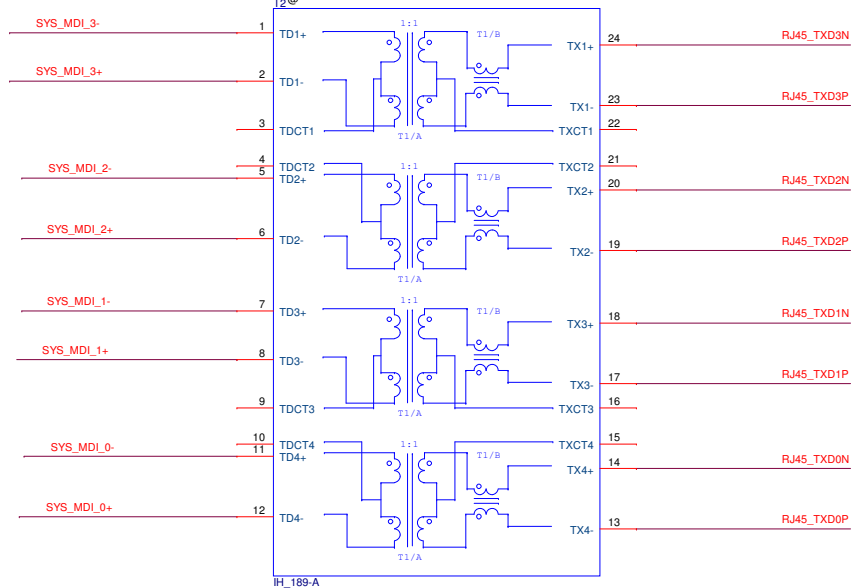
C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

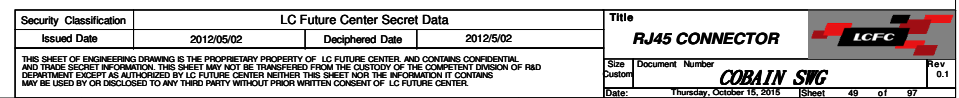
ESD REASON

Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF



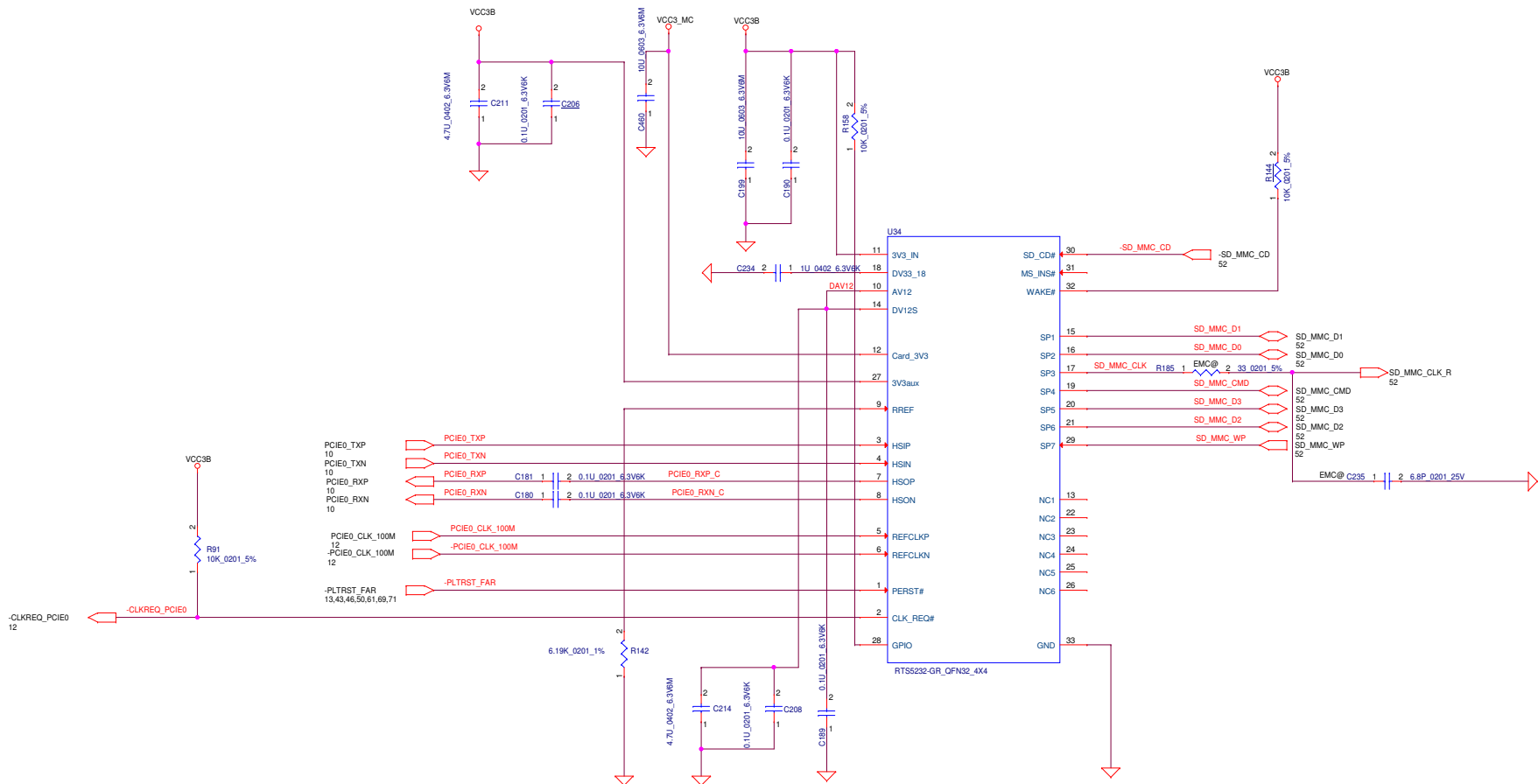
PATTERN MUST BE SHORT AND WIDE.
HIGH VOLTAGE 1500PF CAP IS OPTIONAL

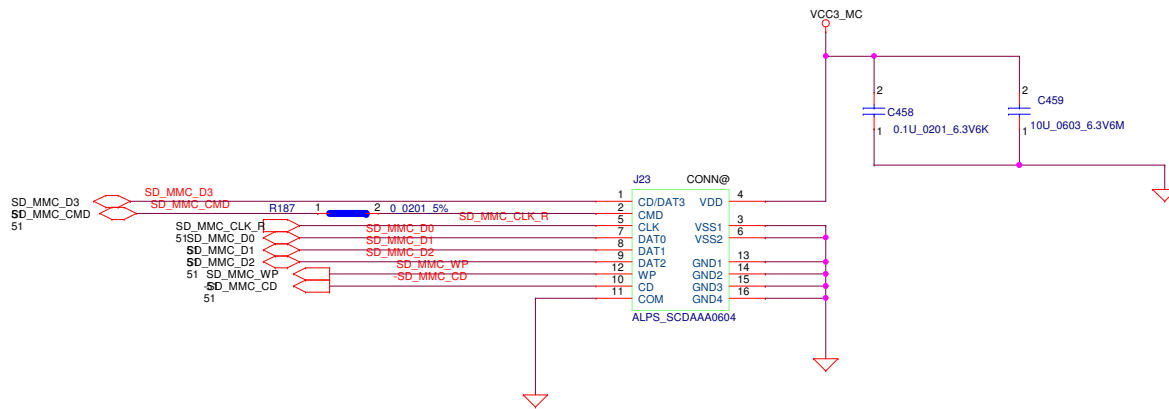


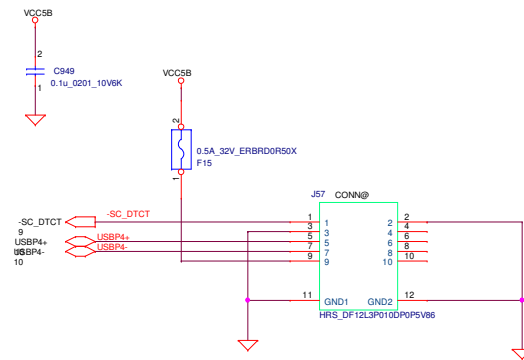


3.2H CONNECTOR

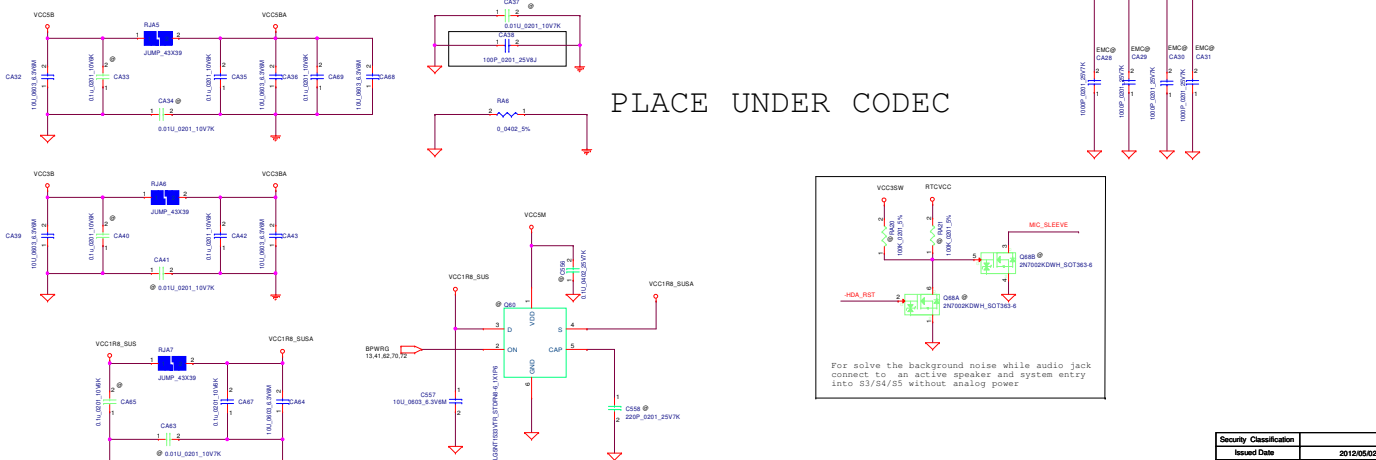




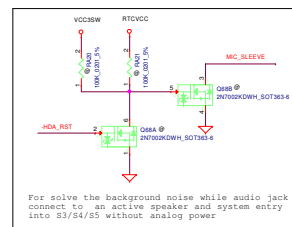




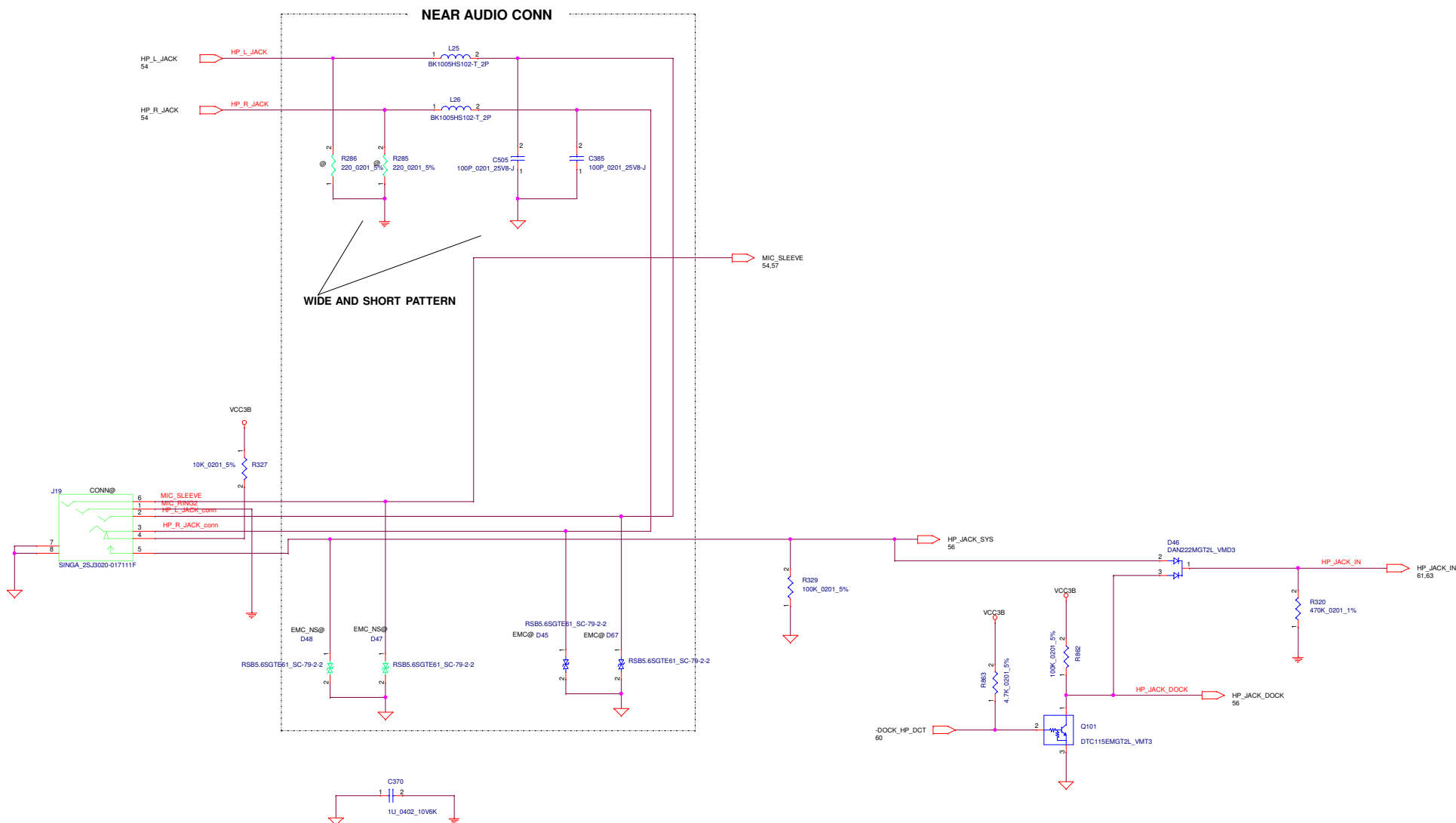
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				Date:	Thursday, October 16, 2013	Sheet 53 of 97




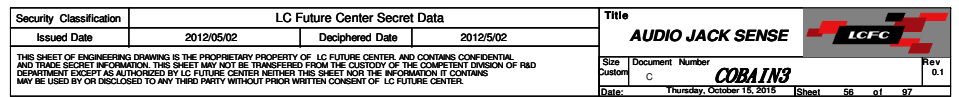
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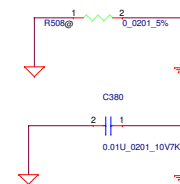
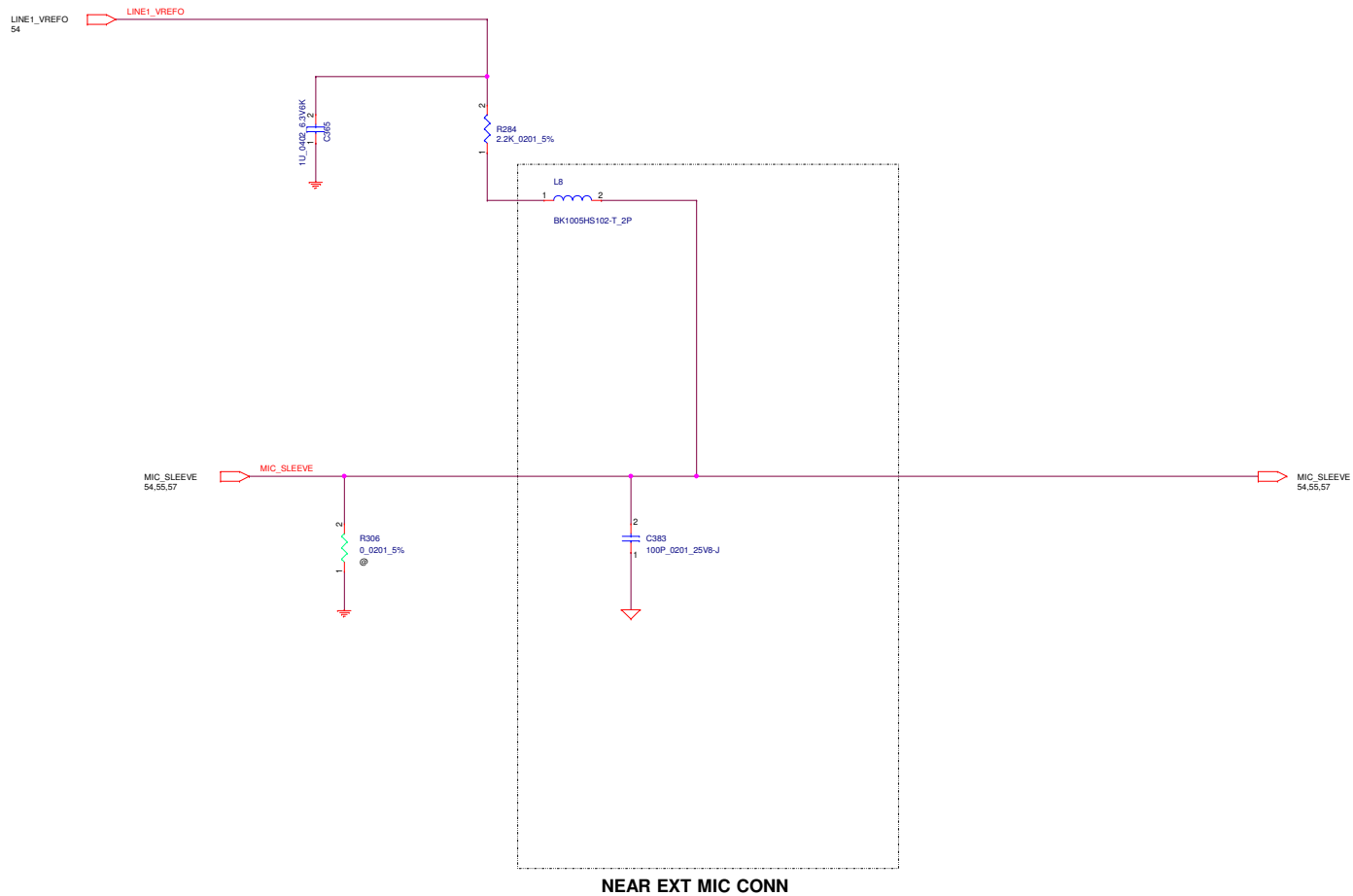


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				COBA1N3		Rev	
				Date		0.1	
				Thursday, October 15, 2015		Sheet 55 of 97	



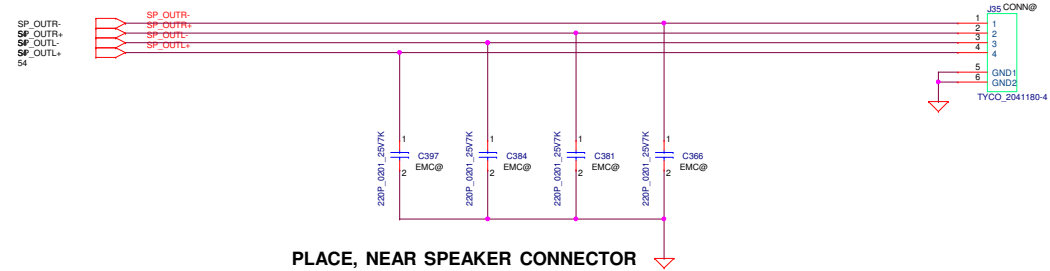


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				Date:	Thursday, October 15, 2015
				Sheet	97 of 97

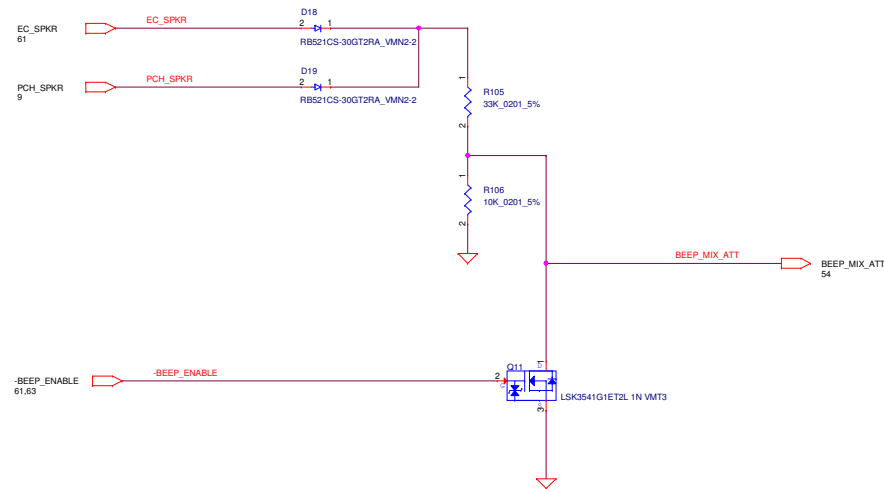


CORAIN SWG

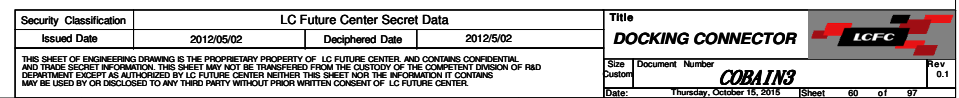
Rev 0.1

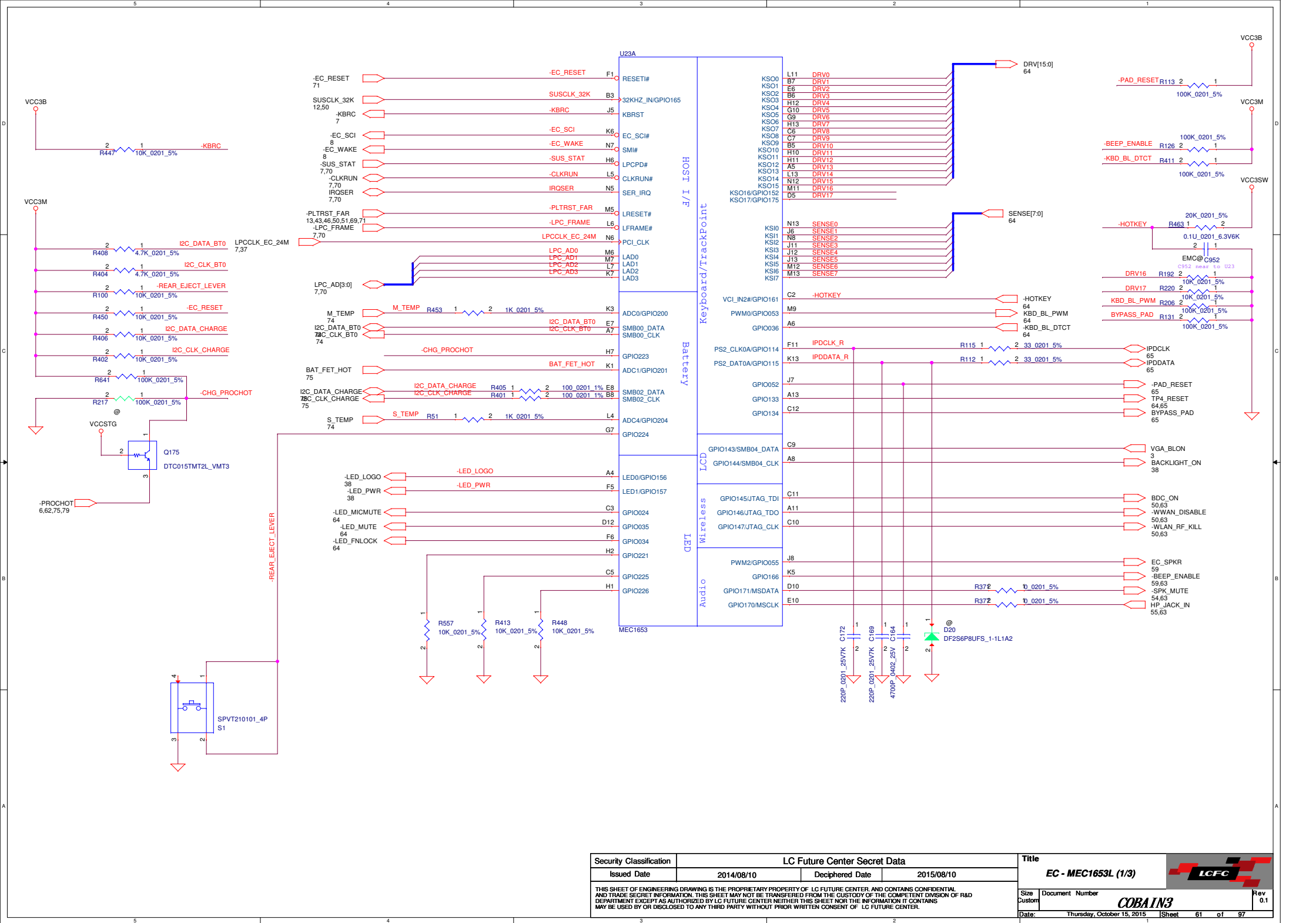


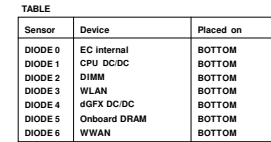
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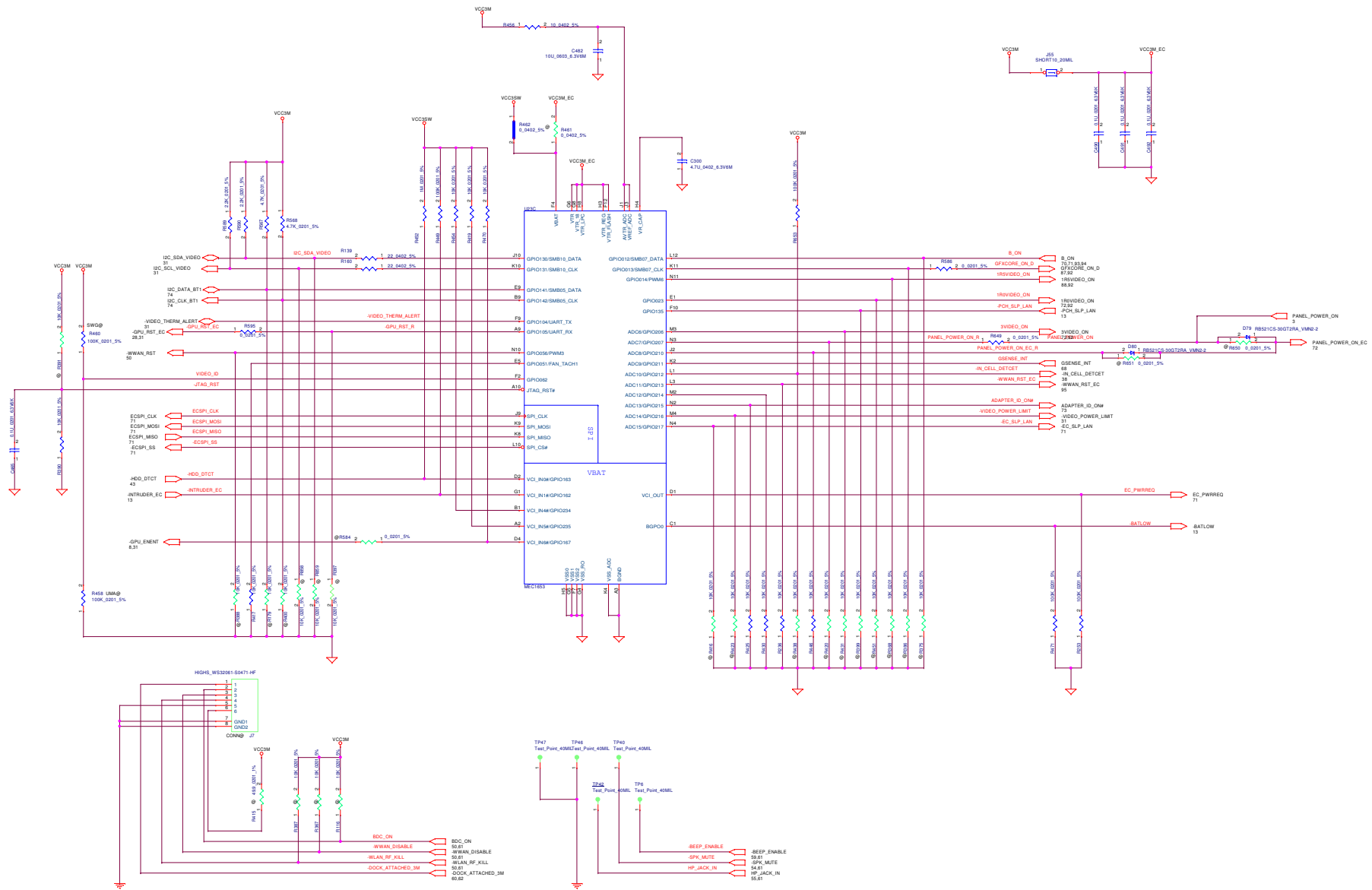


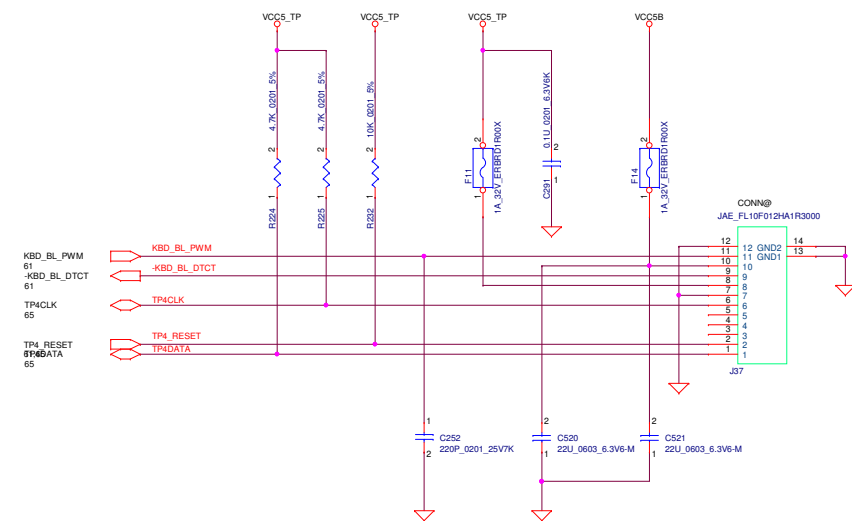
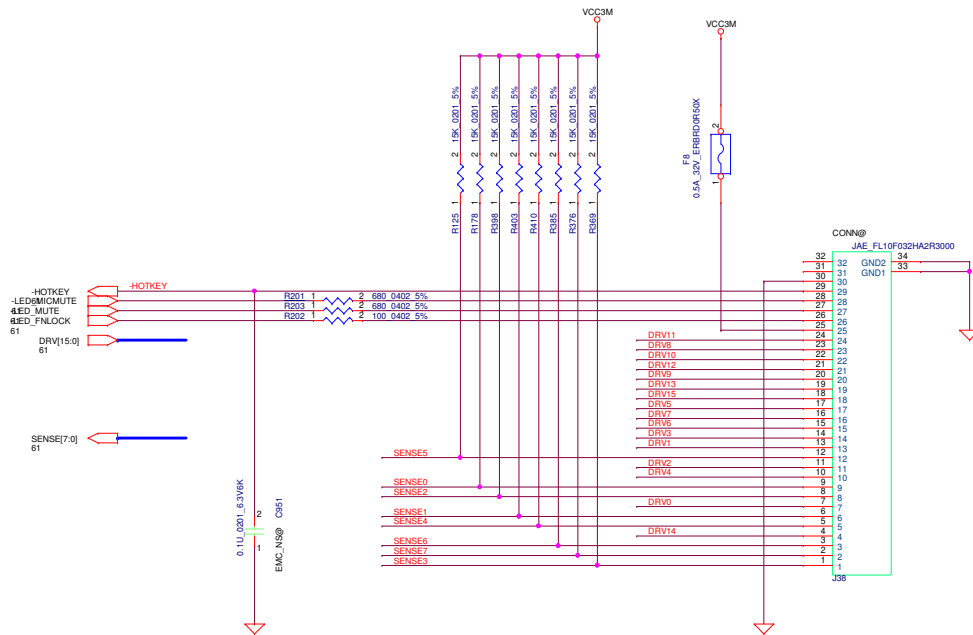
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				Date:	Thursday, October 15, 2015
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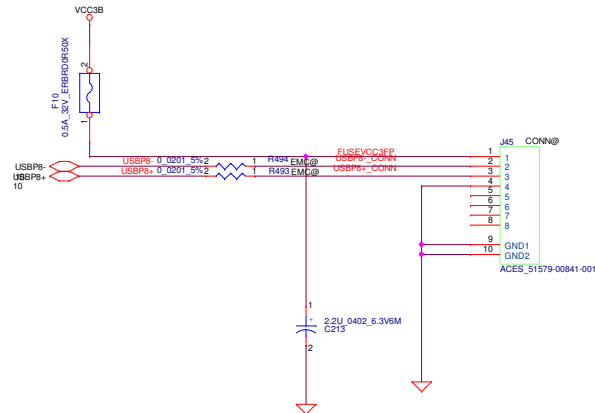
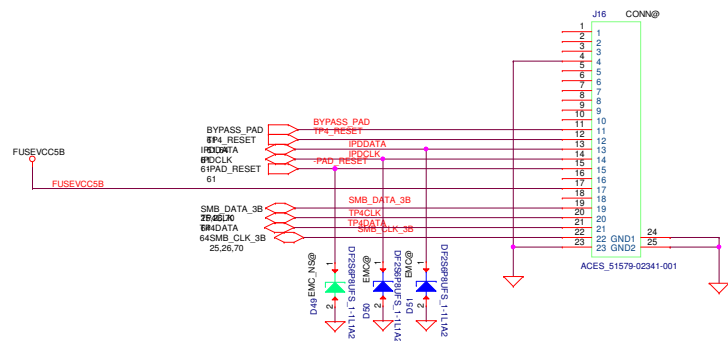
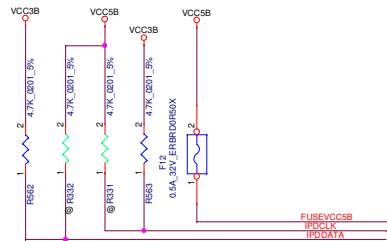






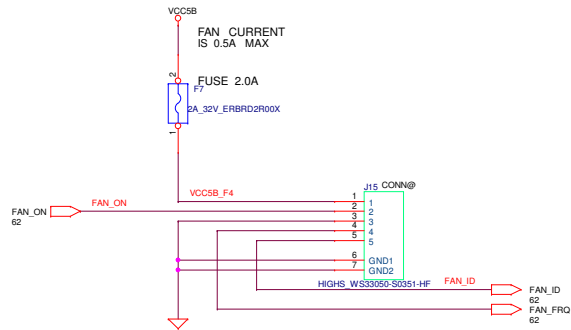







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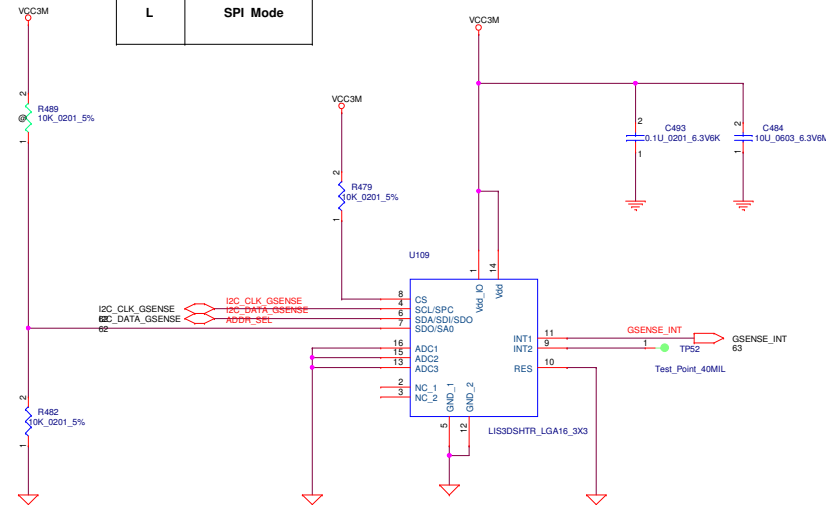
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TABLE

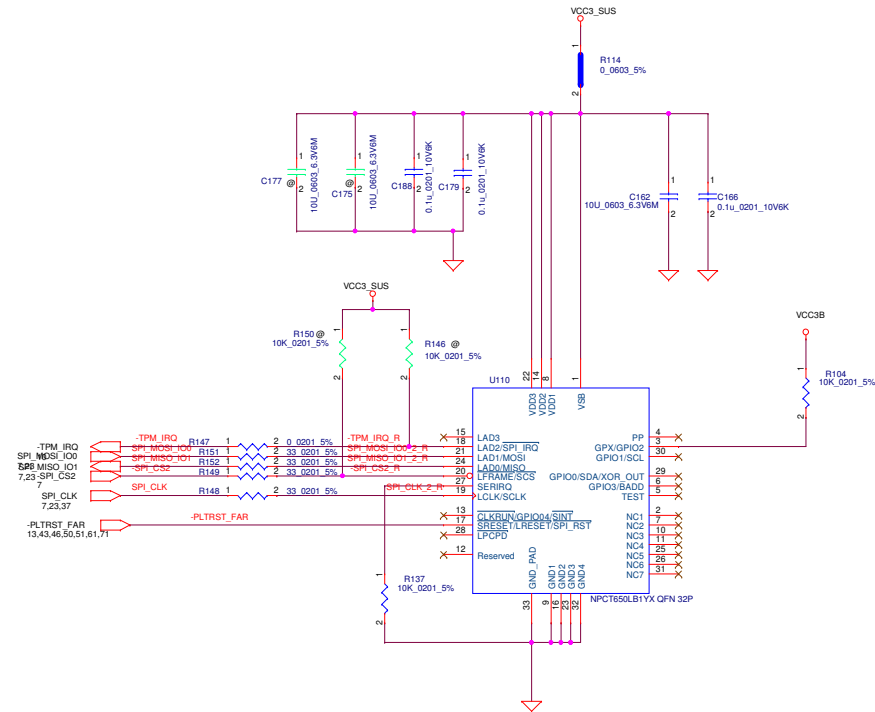
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	L	30h (W) & 31h (R)
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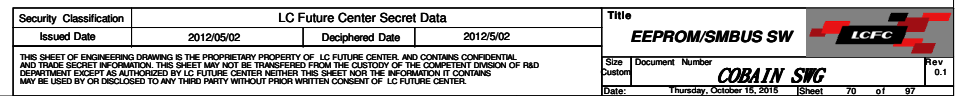
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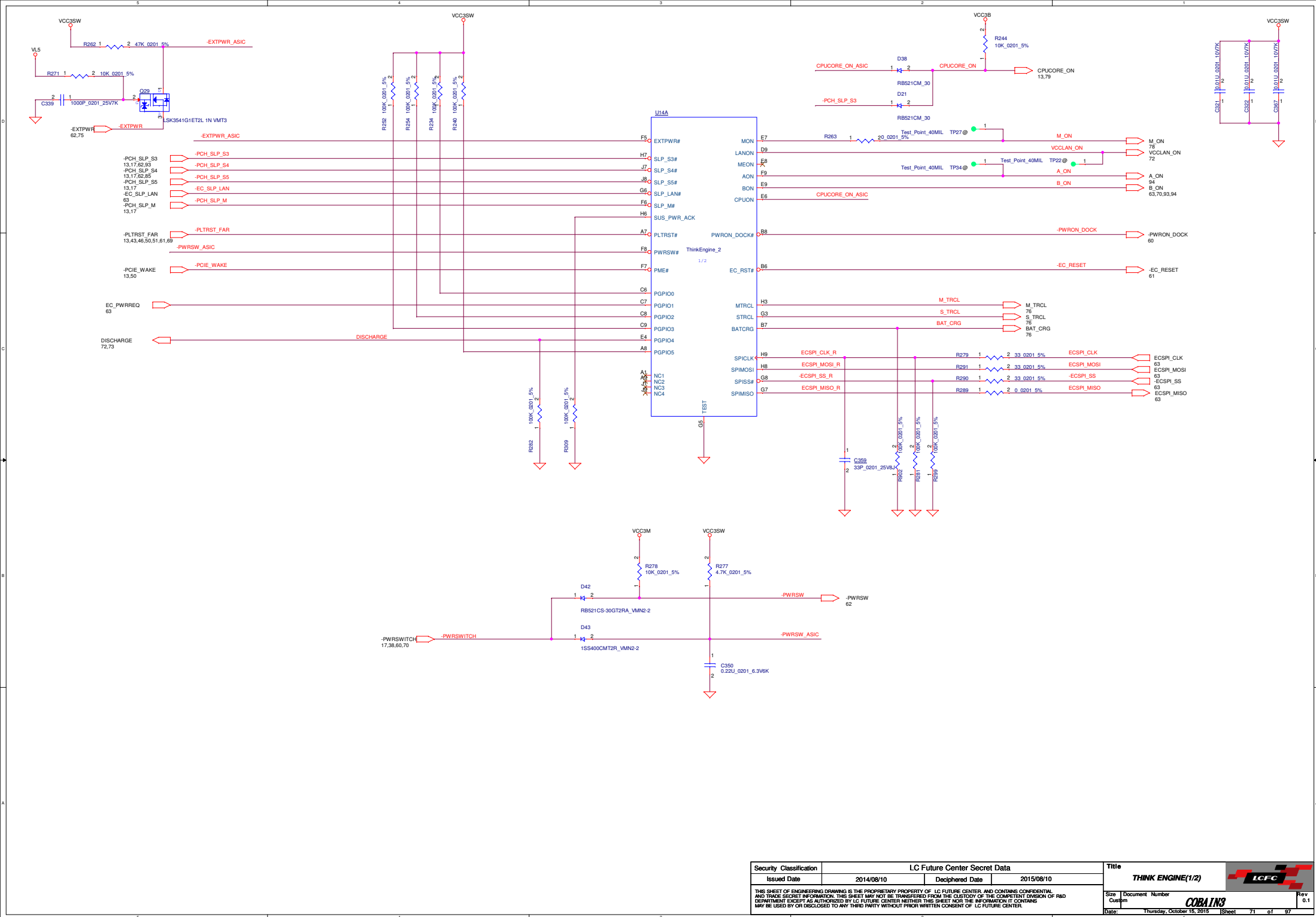


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DCIN

DOCK_PWR20

PLACE NEAR CONNECTOR

DCIN_PWR20_F

VINT20

Total MLCC capacitance at DCIN connector is smaller than 1000pF to avoid LC resonance

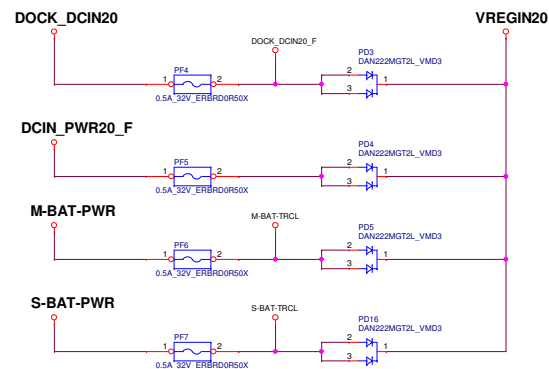
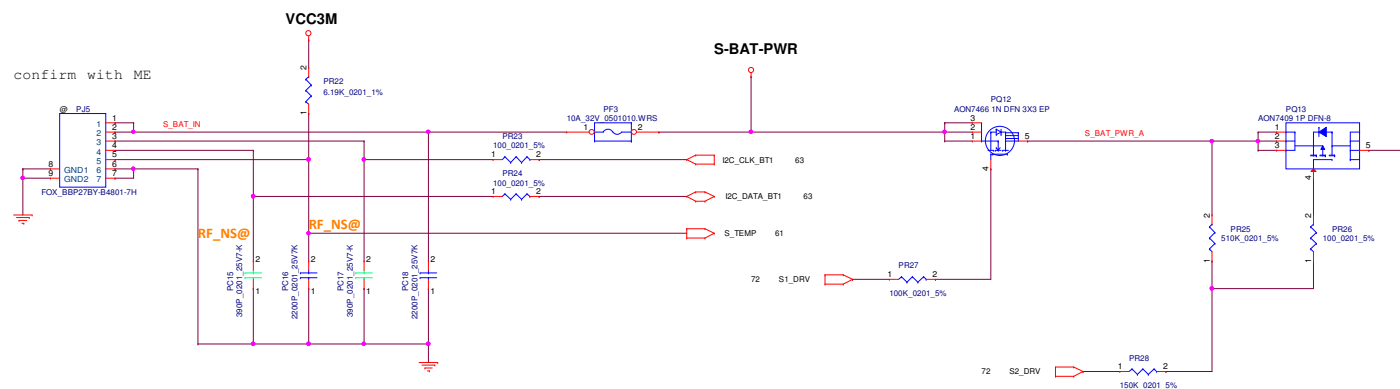
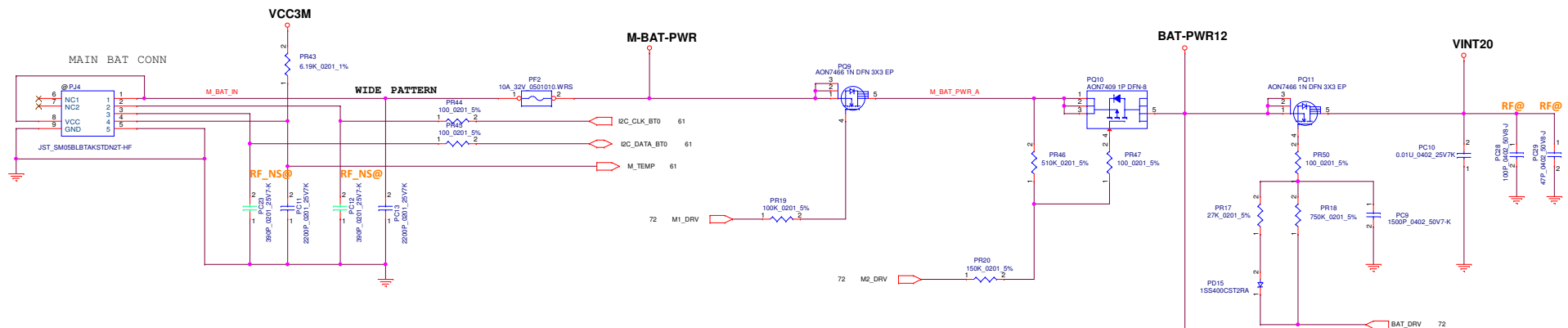
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PR2	ASM	NO-ASM
PQ7	ASM	NO-ASM
PQ6	ASM	NO-ASM

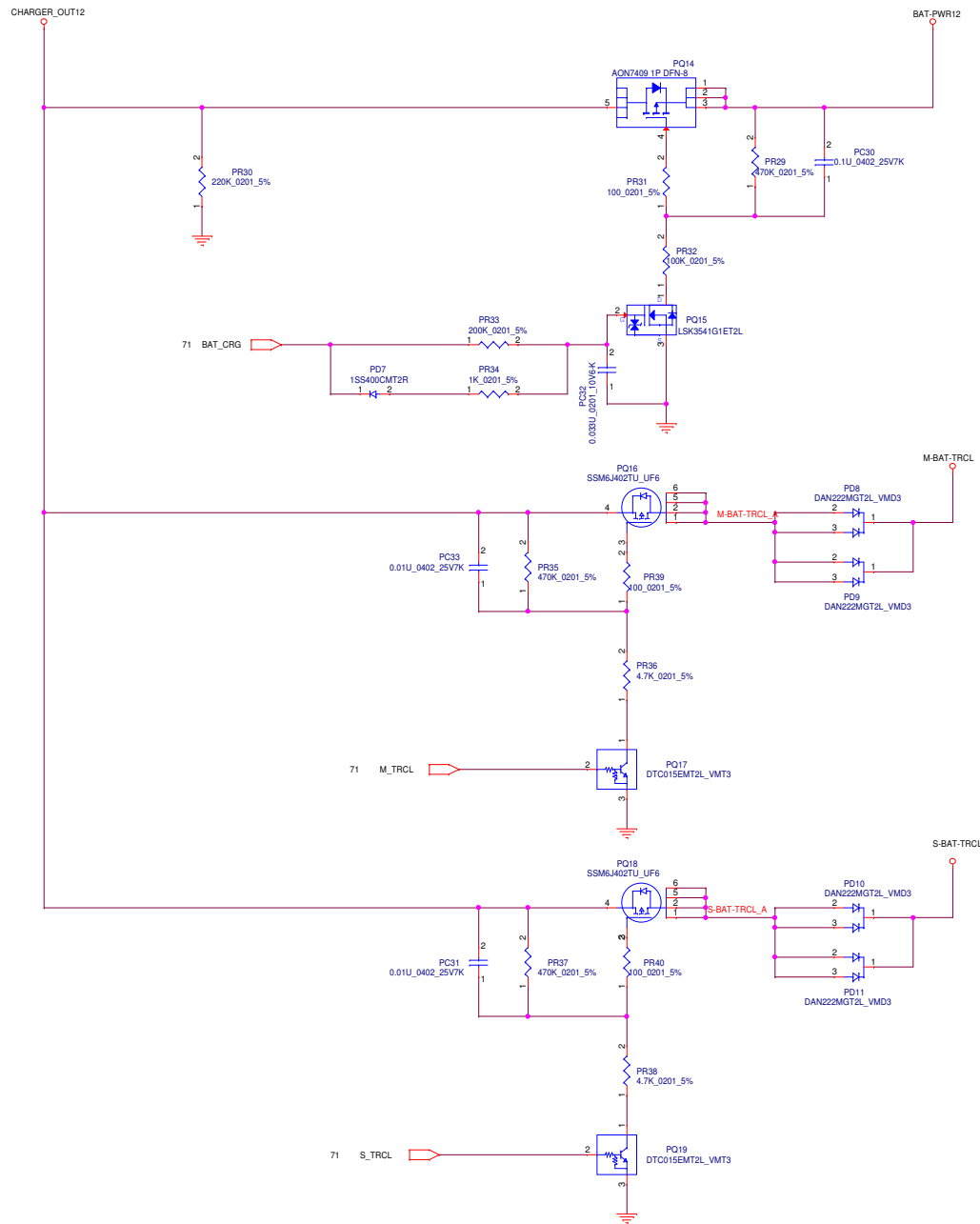
↑
LOGIC


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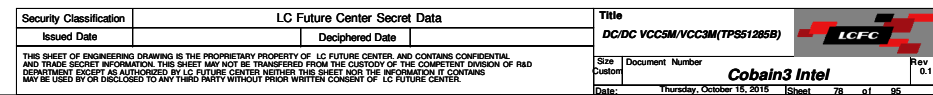


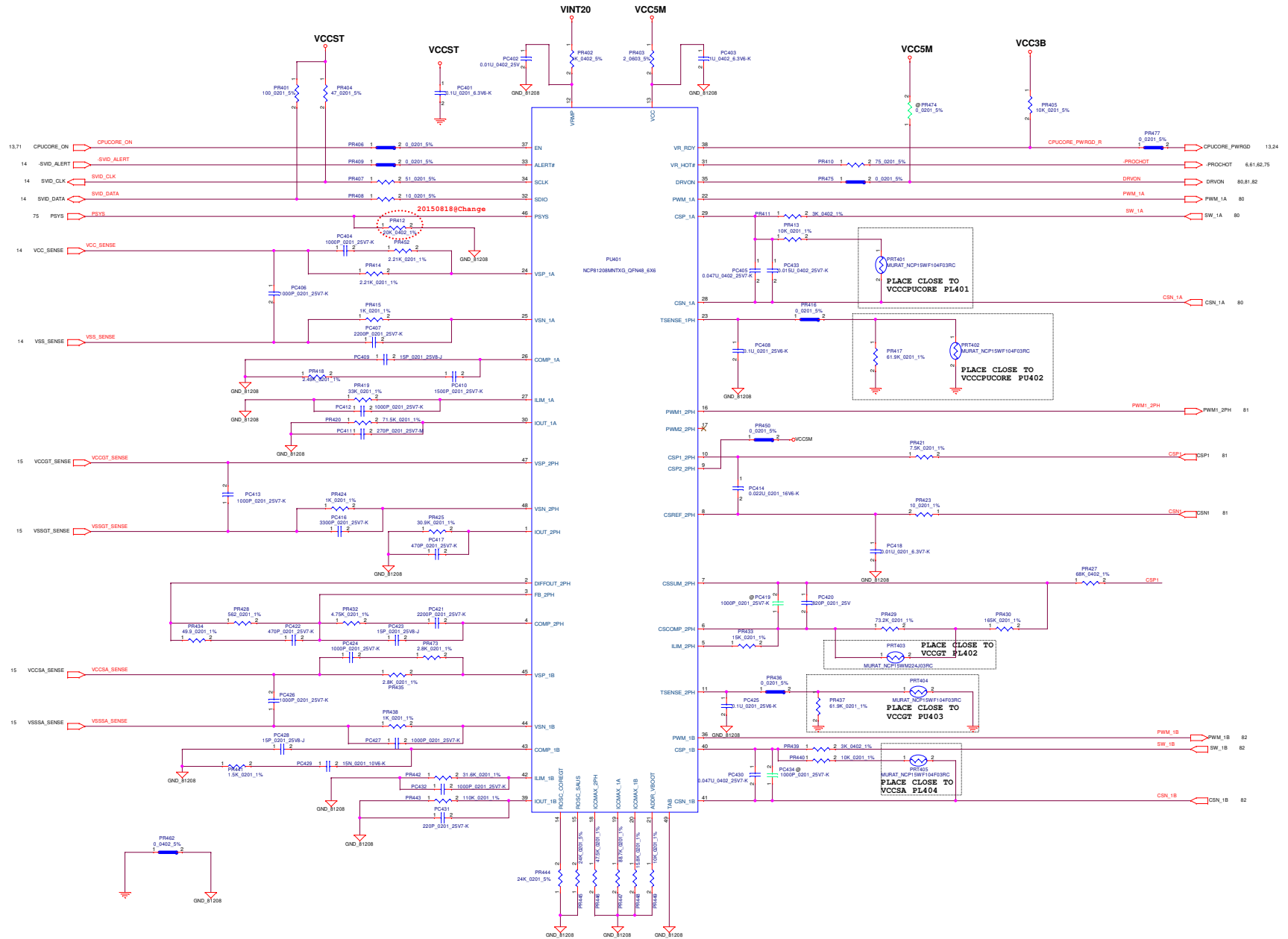
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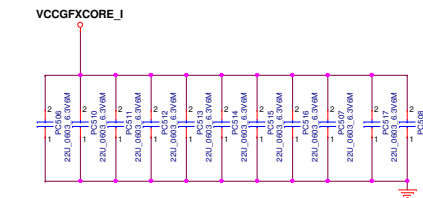
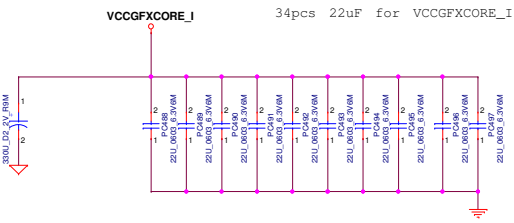
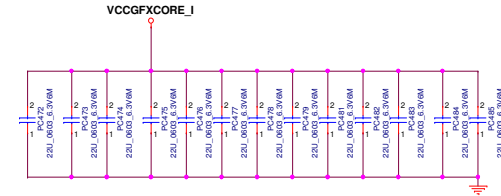
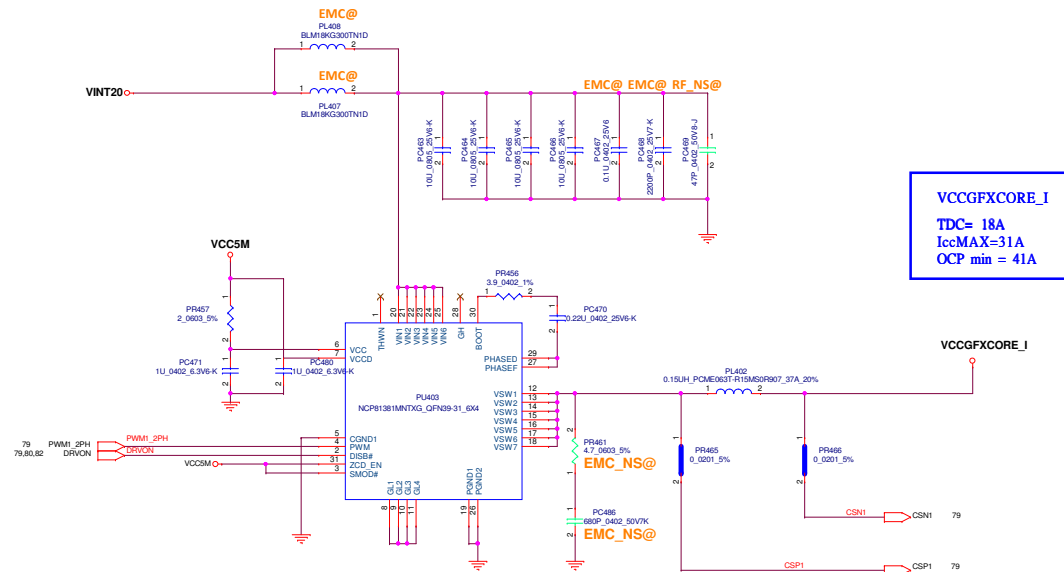
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						Date:	Thursday, October 18, 2018	Sheet	77 of 95

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

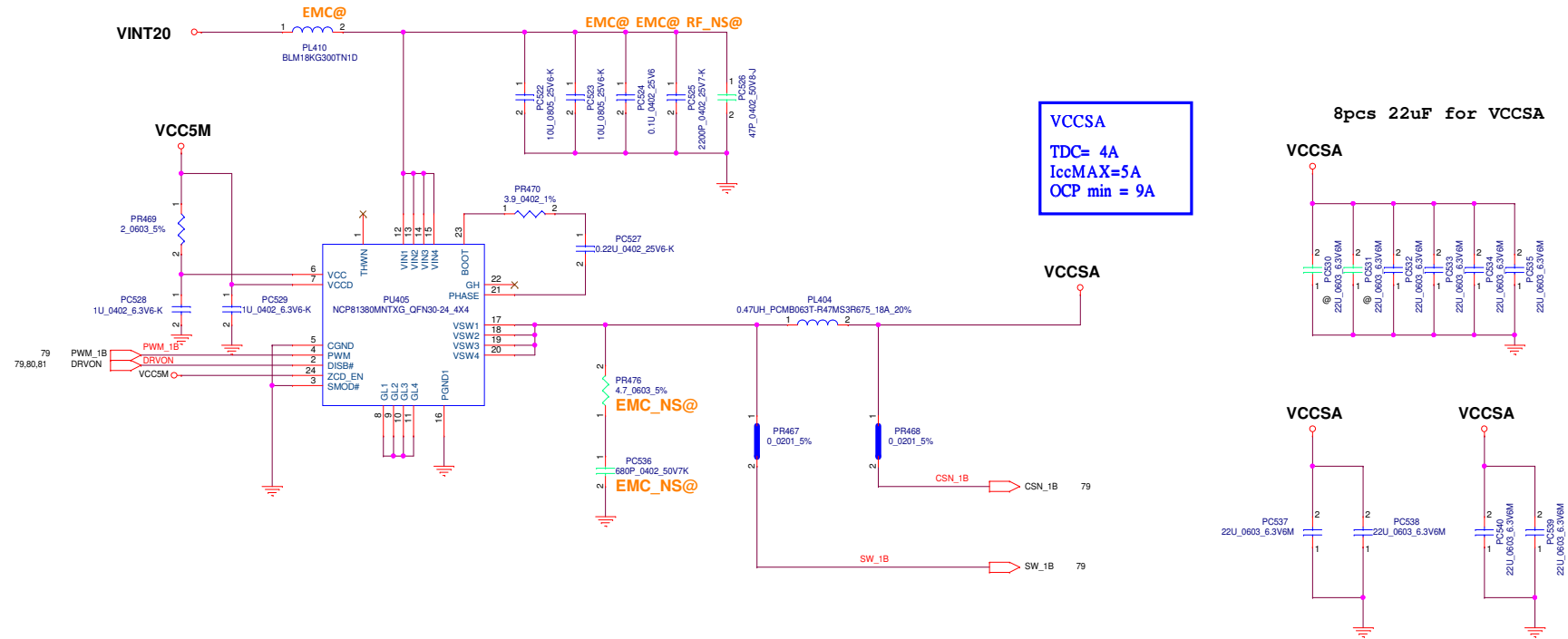






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All the input MLCCs must be placed symmetrically on Top and Bottom.




VCCSA
TDC= 4A
IccMAX=5A
OCP min = 9A

8pcs 22uF for VCCSA

VCCSA


VCCSA

VCCSA

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Size	Document	Number			Rev
Custom		Cobain3 Intel			0.1
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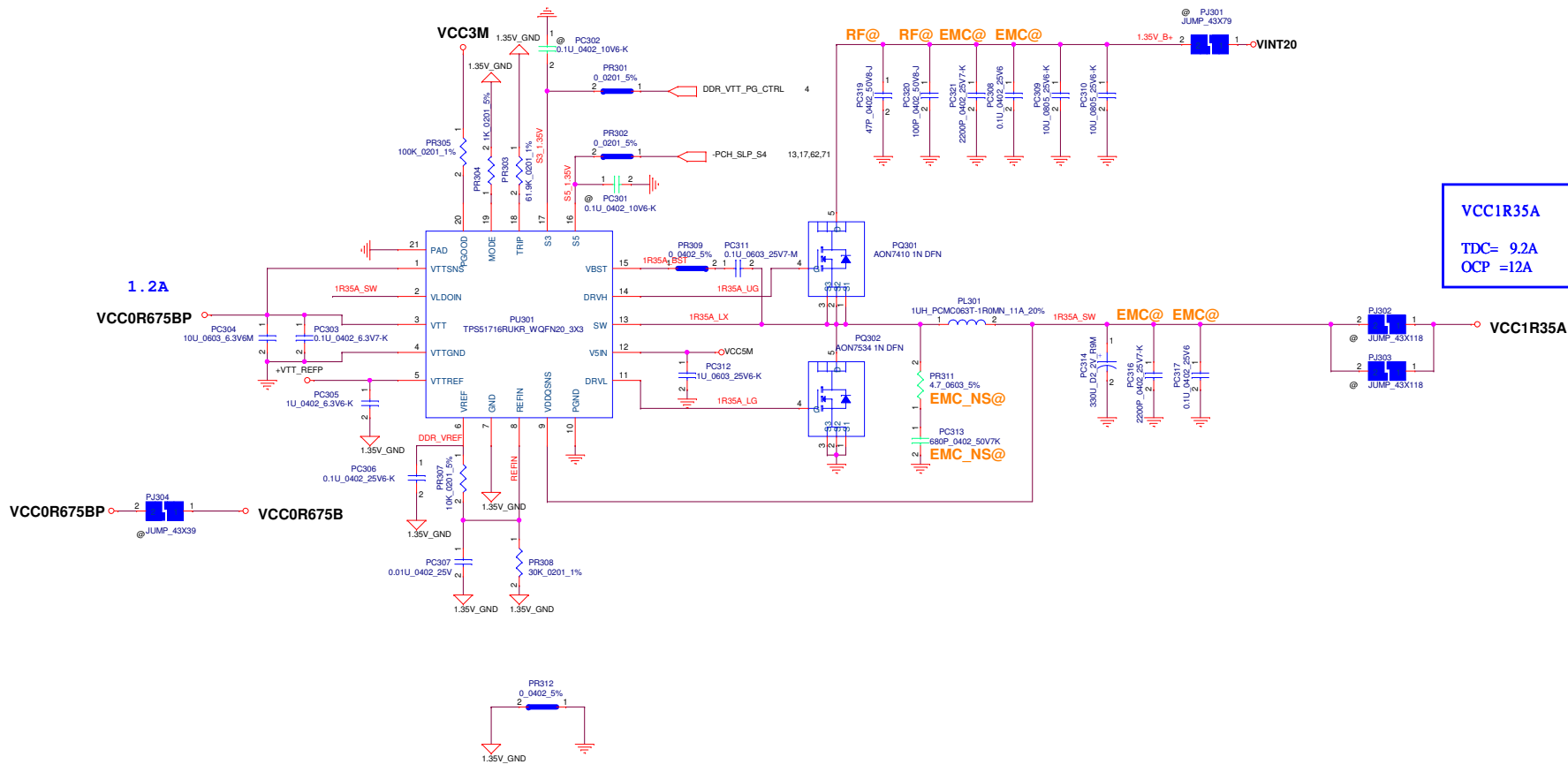
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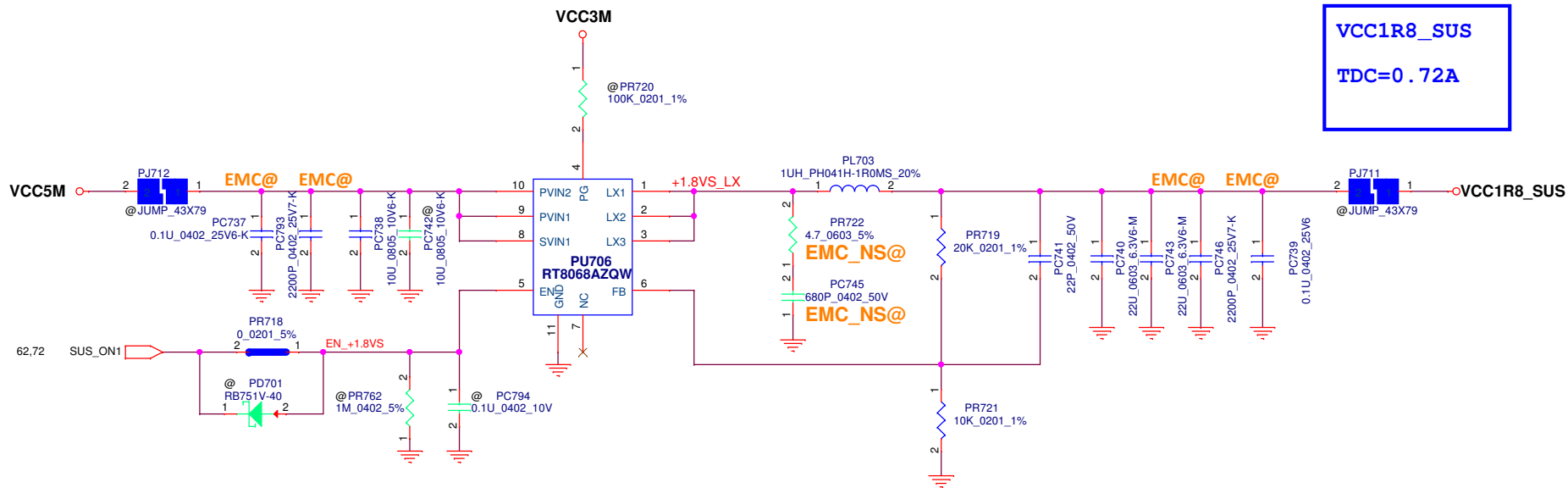
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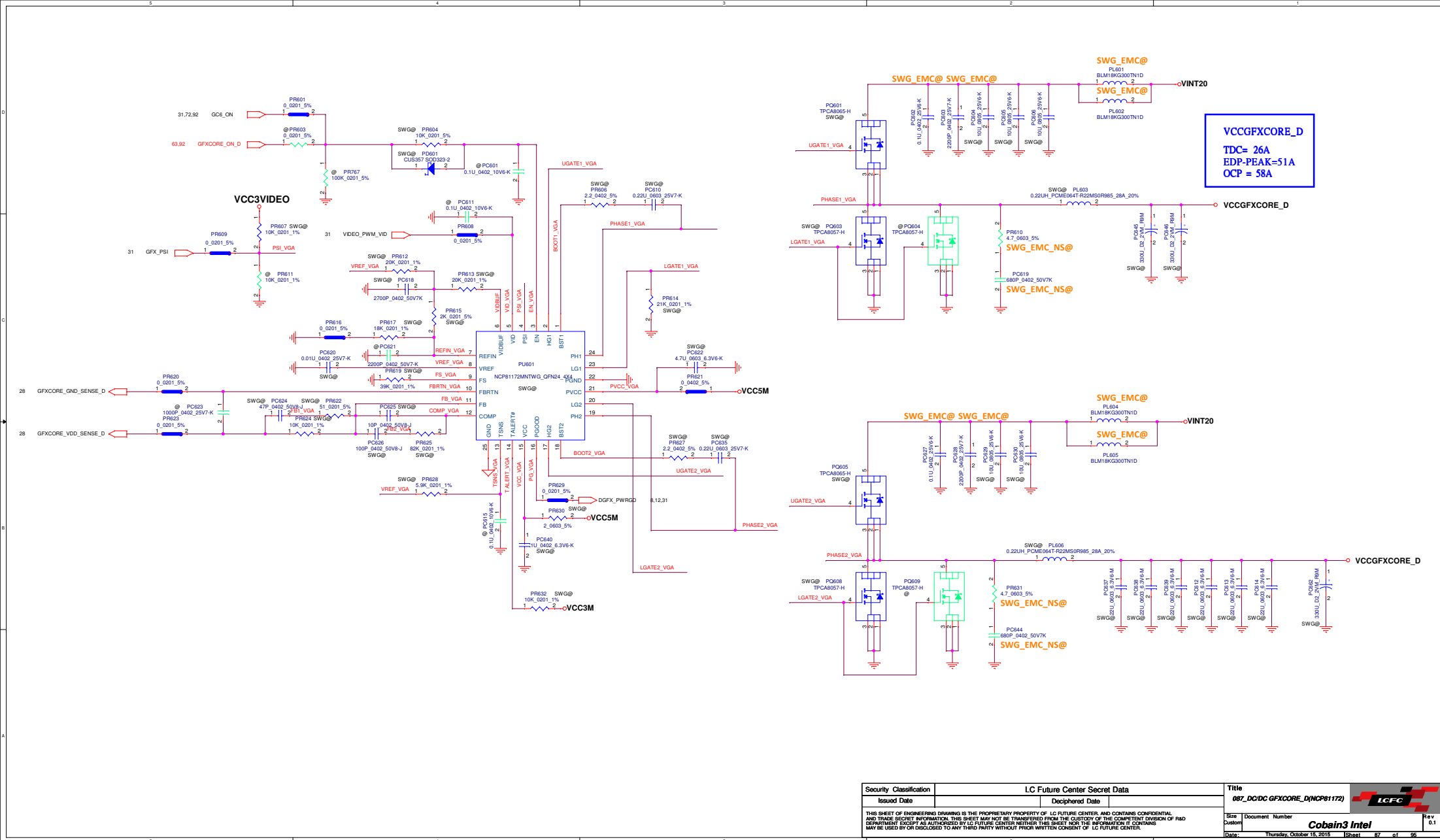


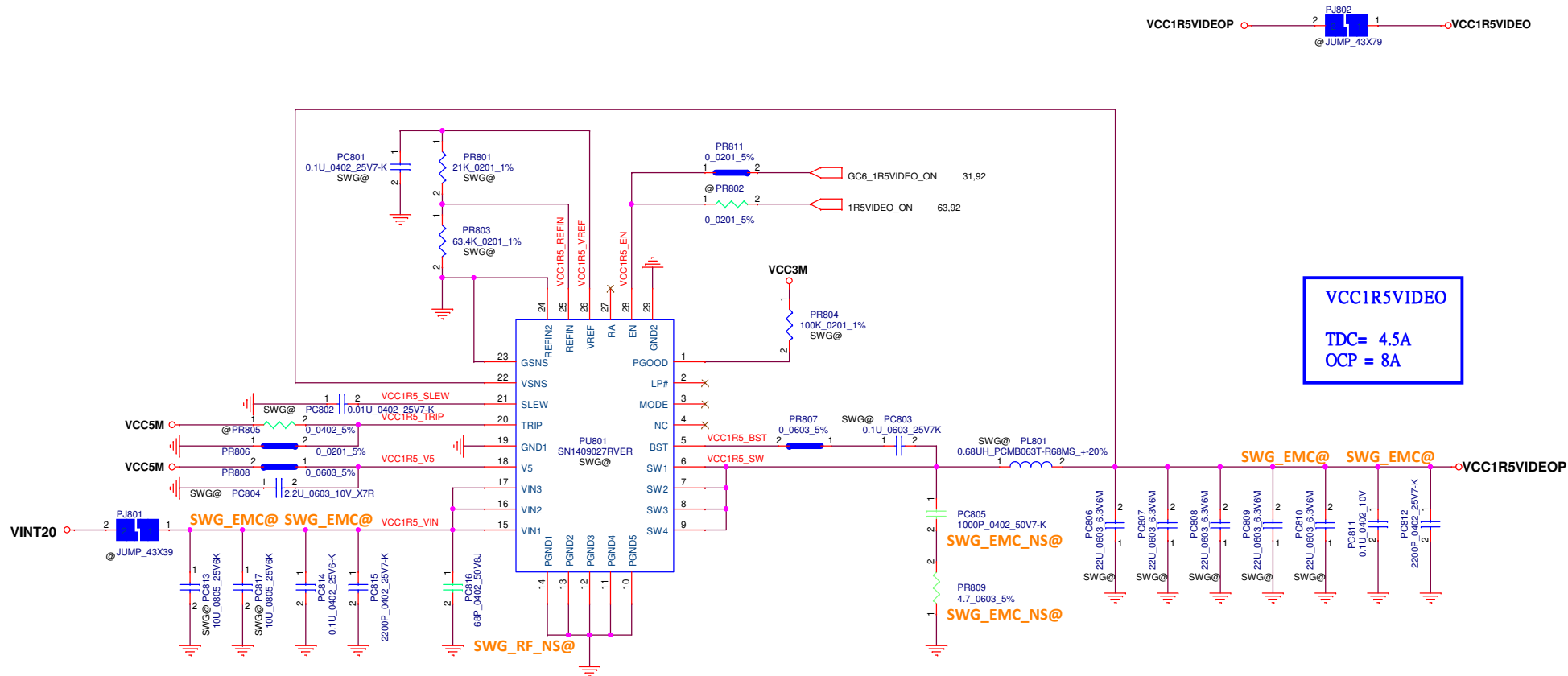
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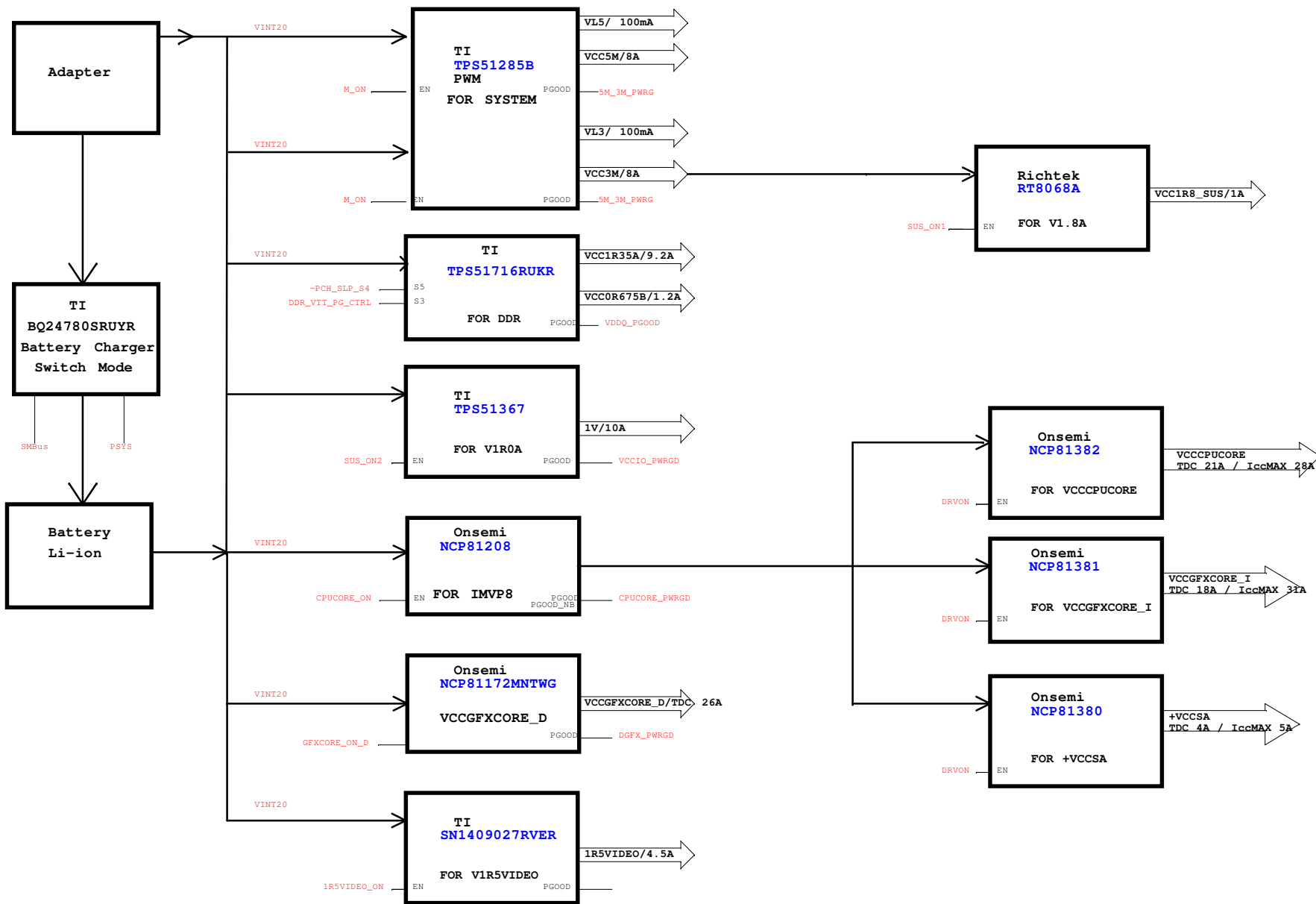


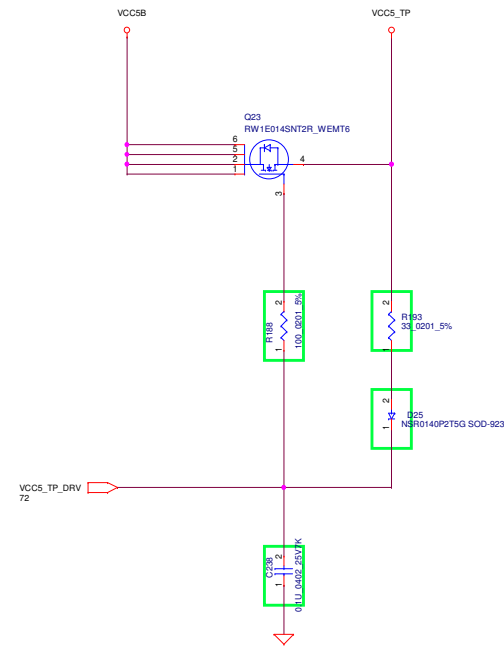
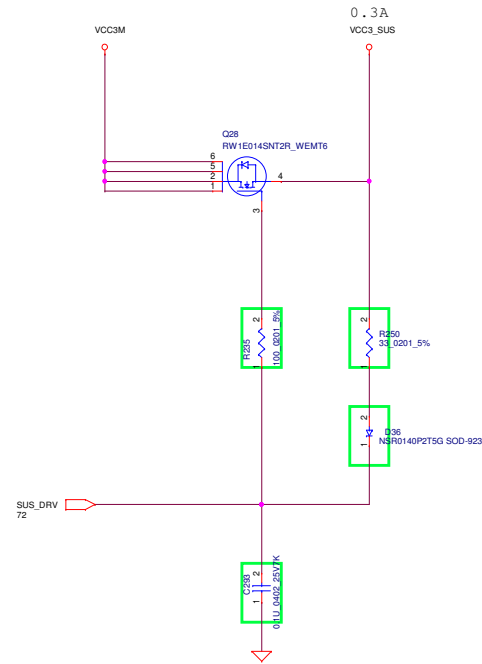
VCC1R5VIDEO

TDC= 4.5A

OCP = 8A

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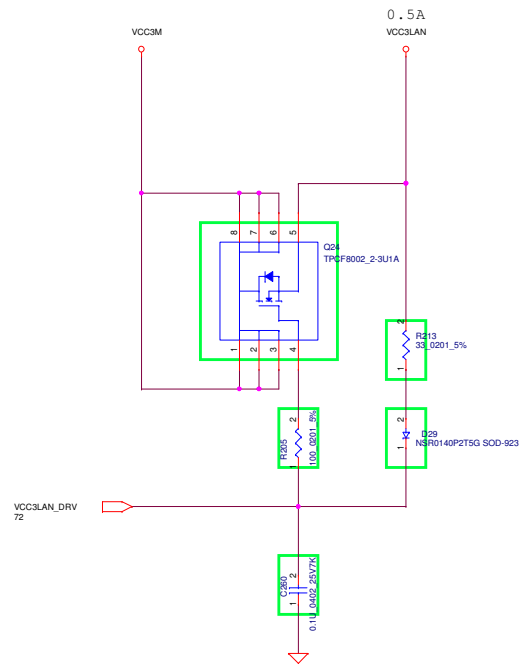




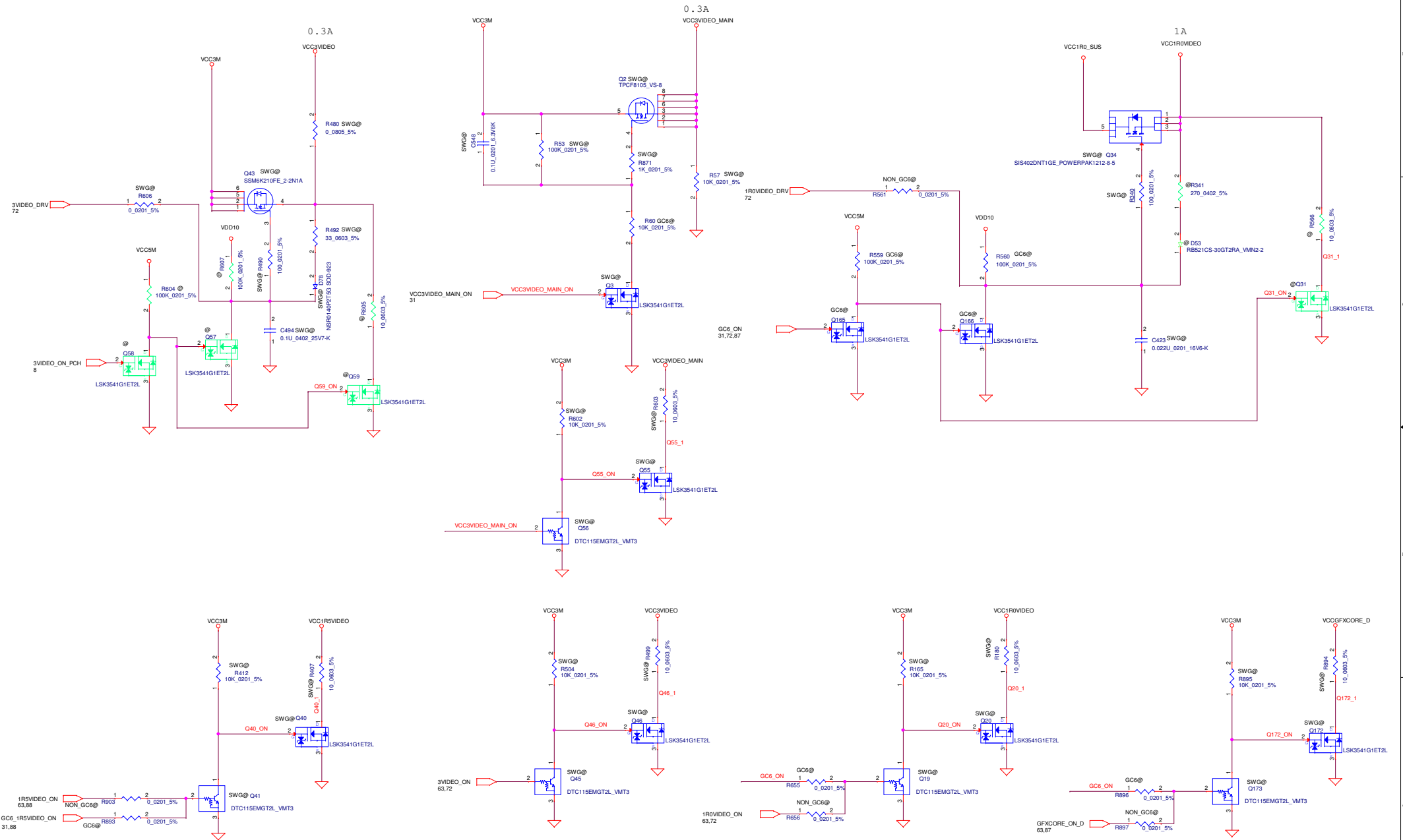
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				Date: Thursday, October 18, 2018	0.24
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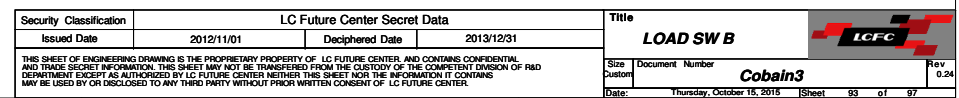
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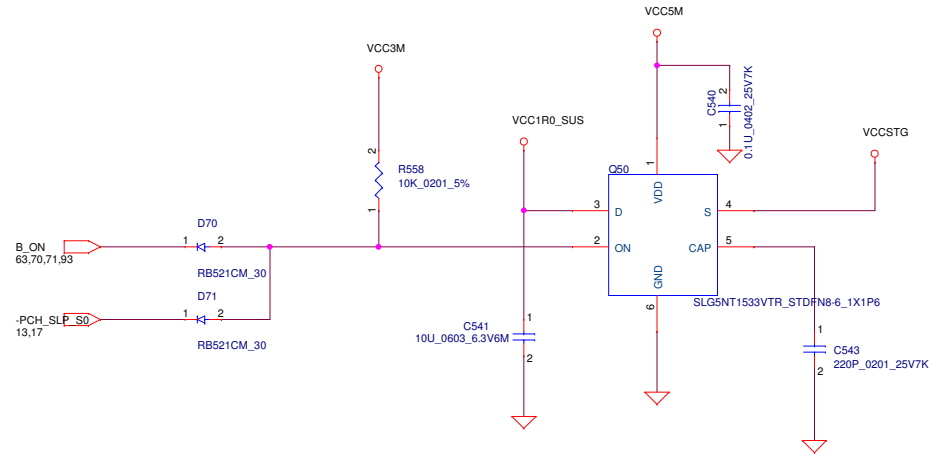
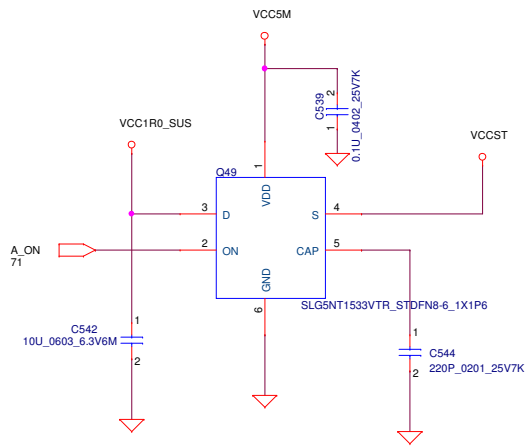


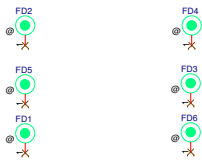
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FID	
Component	Area

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